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S9500-22XST DCSG

4*1G RJ45 / 8*10G SFP+ / 8*25G SFP28 /2*100G QSFP28 with SyncE & 1588V2 Support

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<Variant Name>

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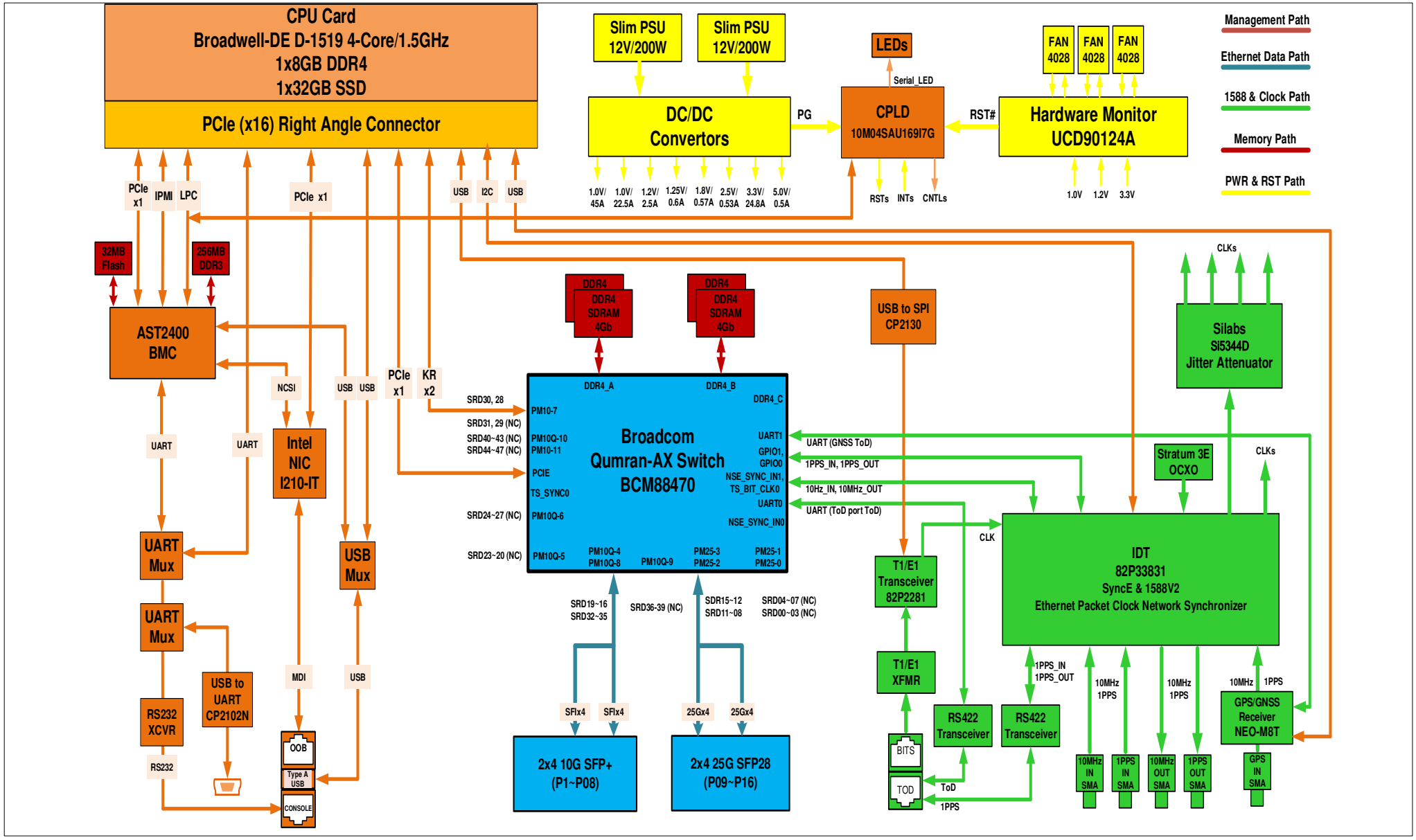
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S9500-22XST DCSG DESIGN CHANGE HISTORY

Change History
Please refer Page 76 and Page 77

SYSTEM BLOCK DIAGRAM



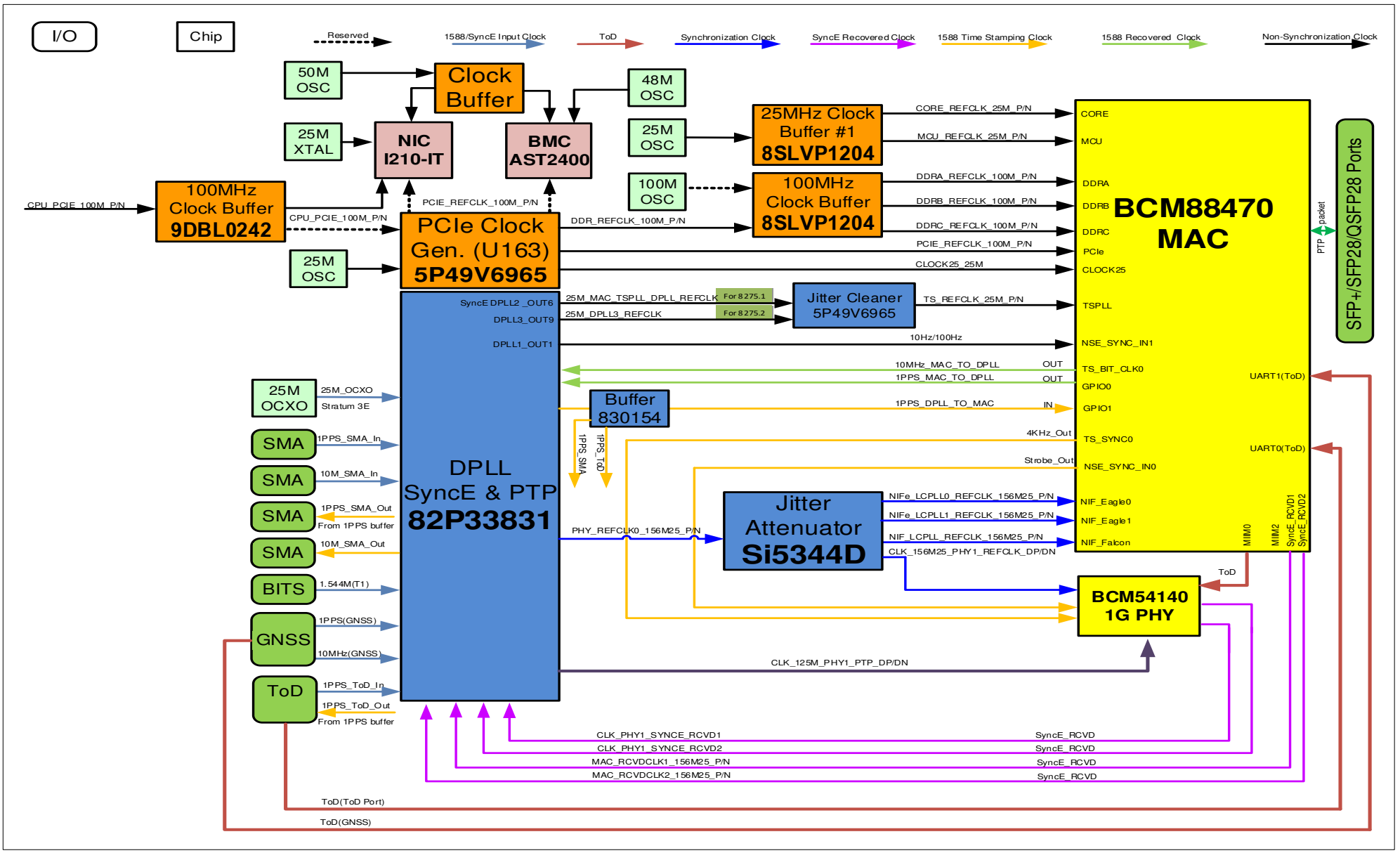
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Title: 03. SYSTEM BLOCK DIAGRAM

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CLOCK BLOCK DIAGRAM



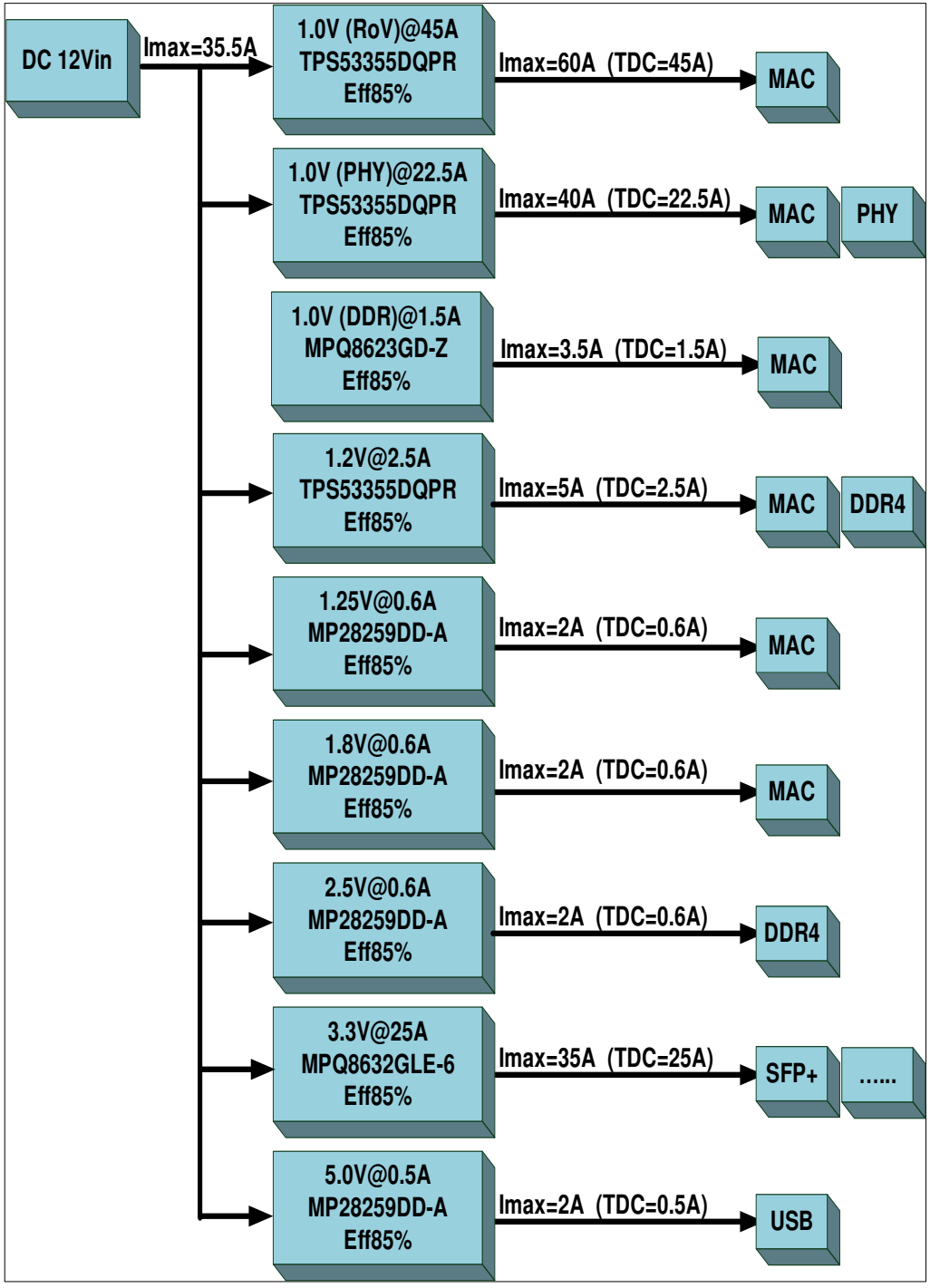
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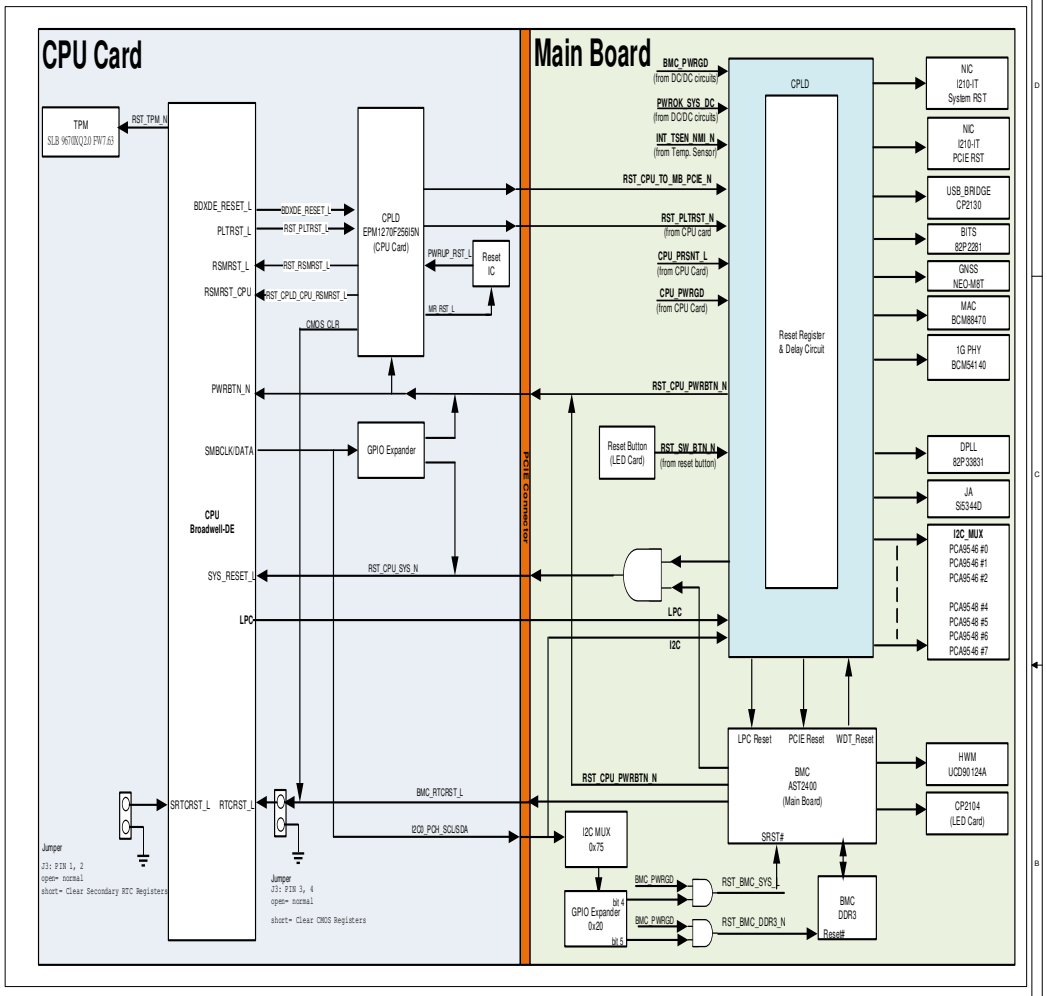
ufiSpace UfiSpace Co., Ltd.

Title: 04. CLOCK BLOCK DIAGRAM

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PWR & RST BLOCK DIAGRAM





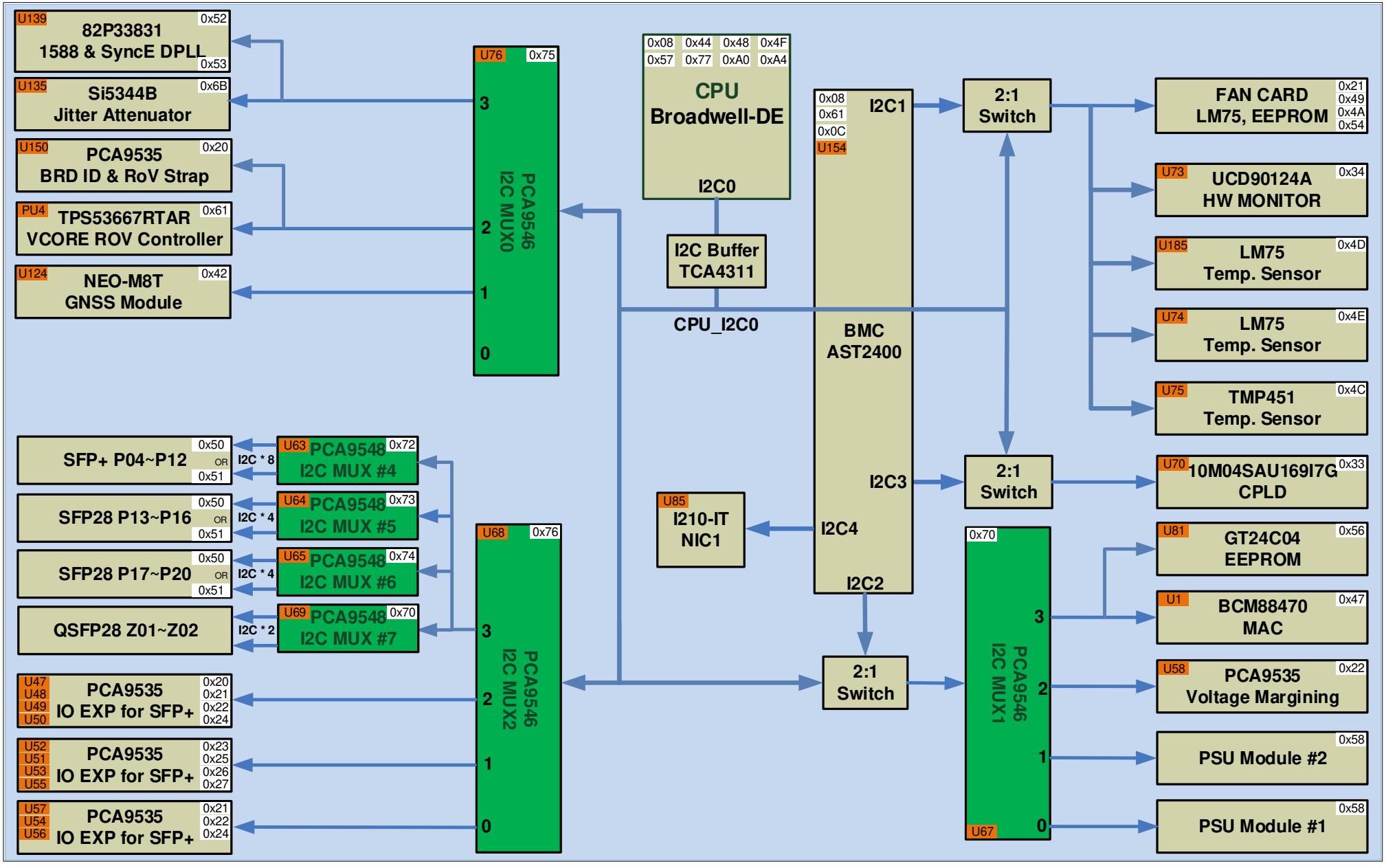
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Title: 05. PWR & RST BLOCK DIAGRAM

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I2C & JTAG BLOCK DIAGRAM



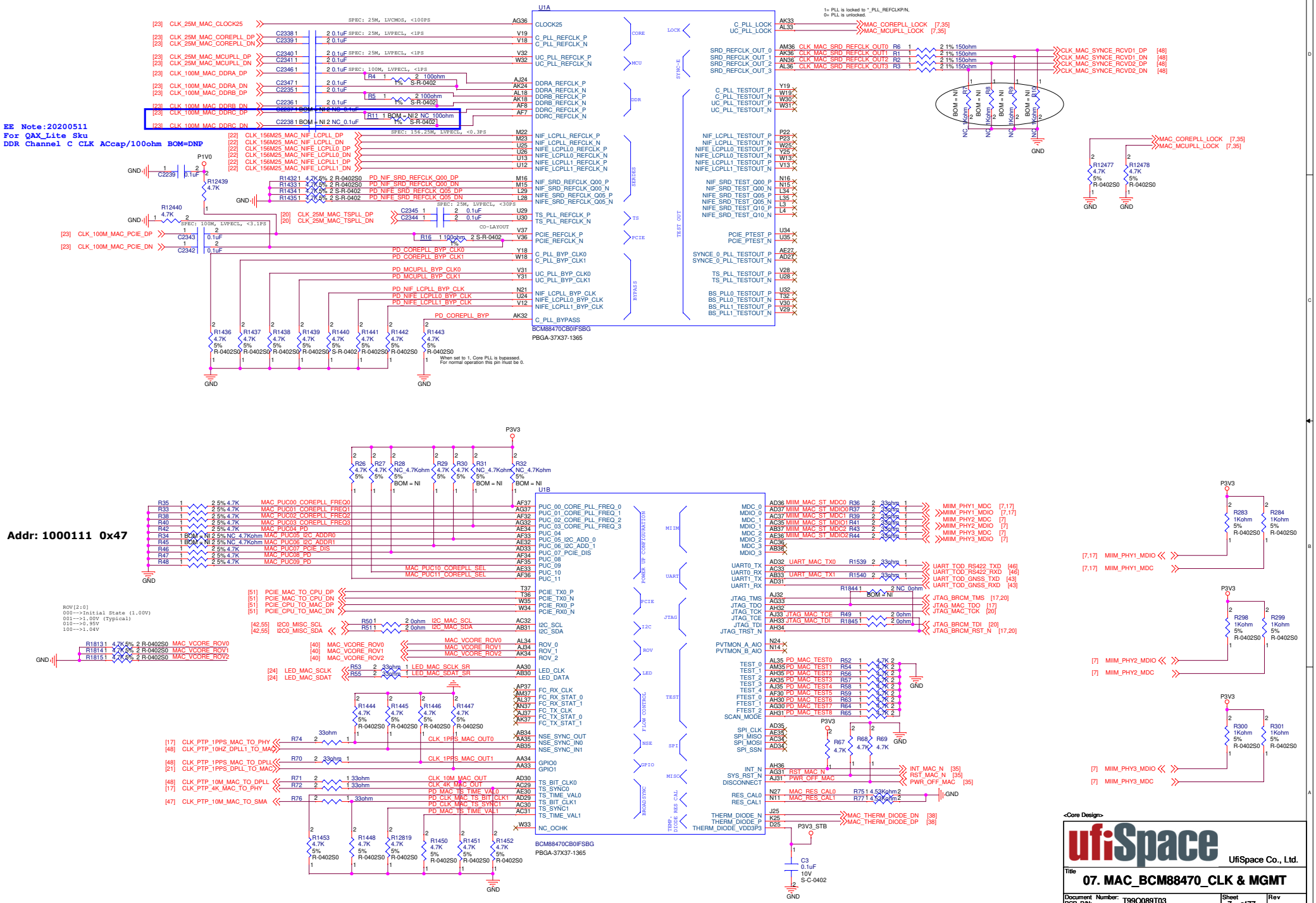
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Title: 06. I2C & JTAG BLOCK DIAGRAM

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MAC_BCM88470_CLK & MGMT



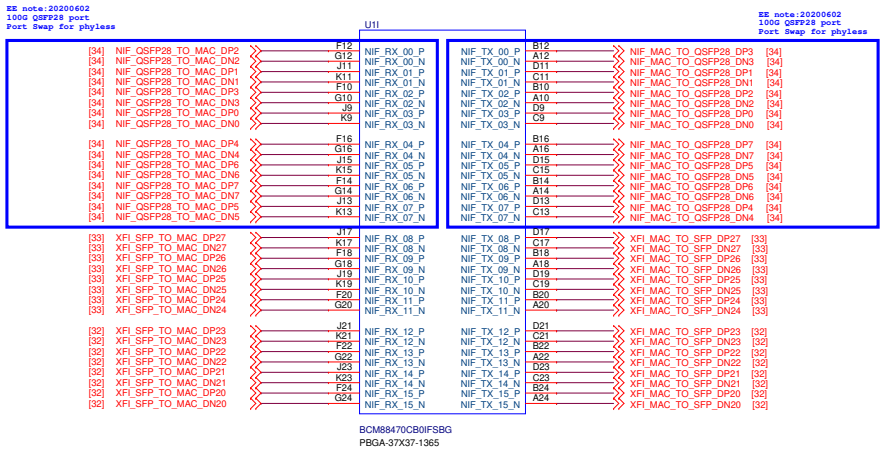
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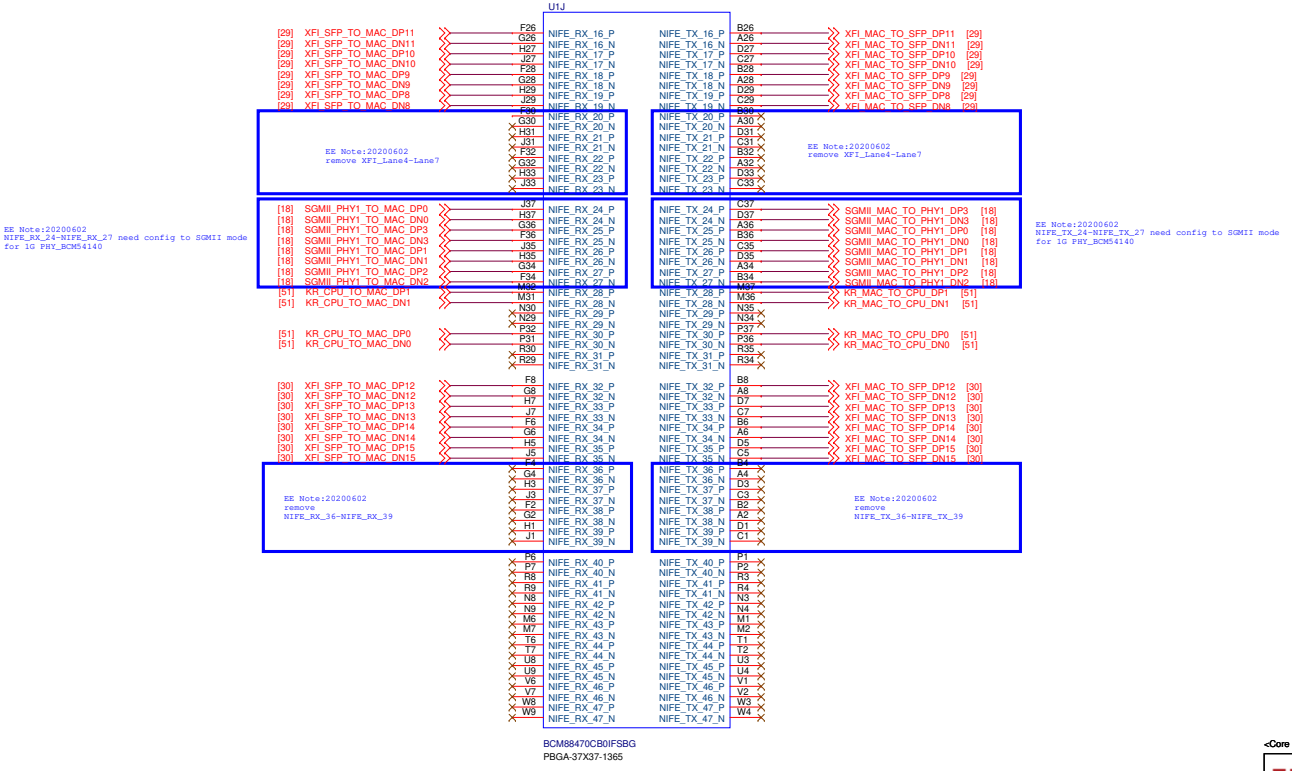
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Title: 07. MAC_BCM88470_CLK & MGMT

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MAC_BCM88470_SERDES





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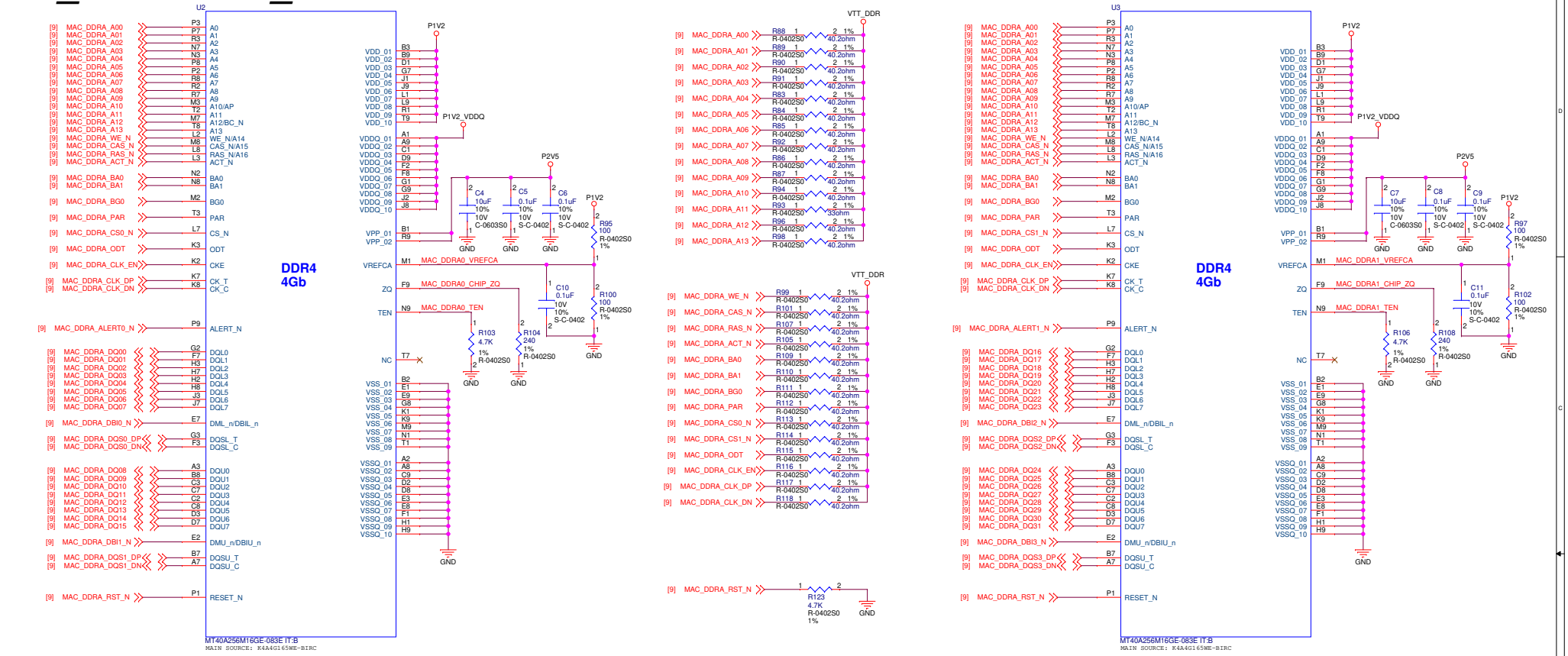
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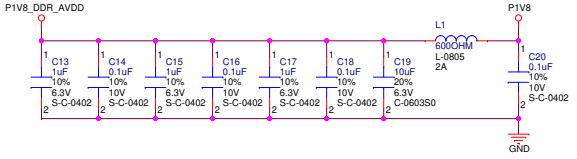
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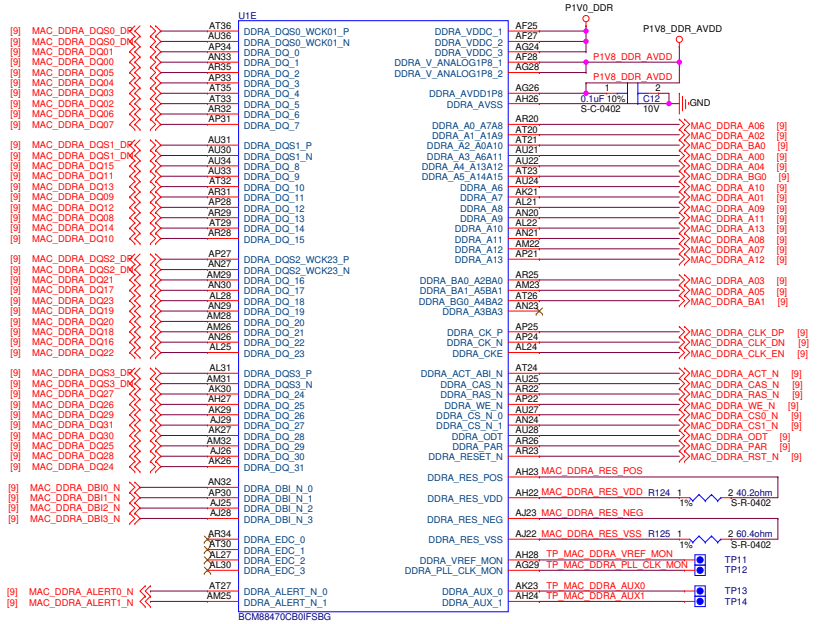
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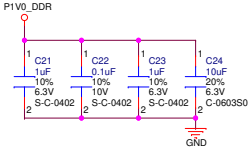
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MAC_BCM88470_DDRA & SDRAM







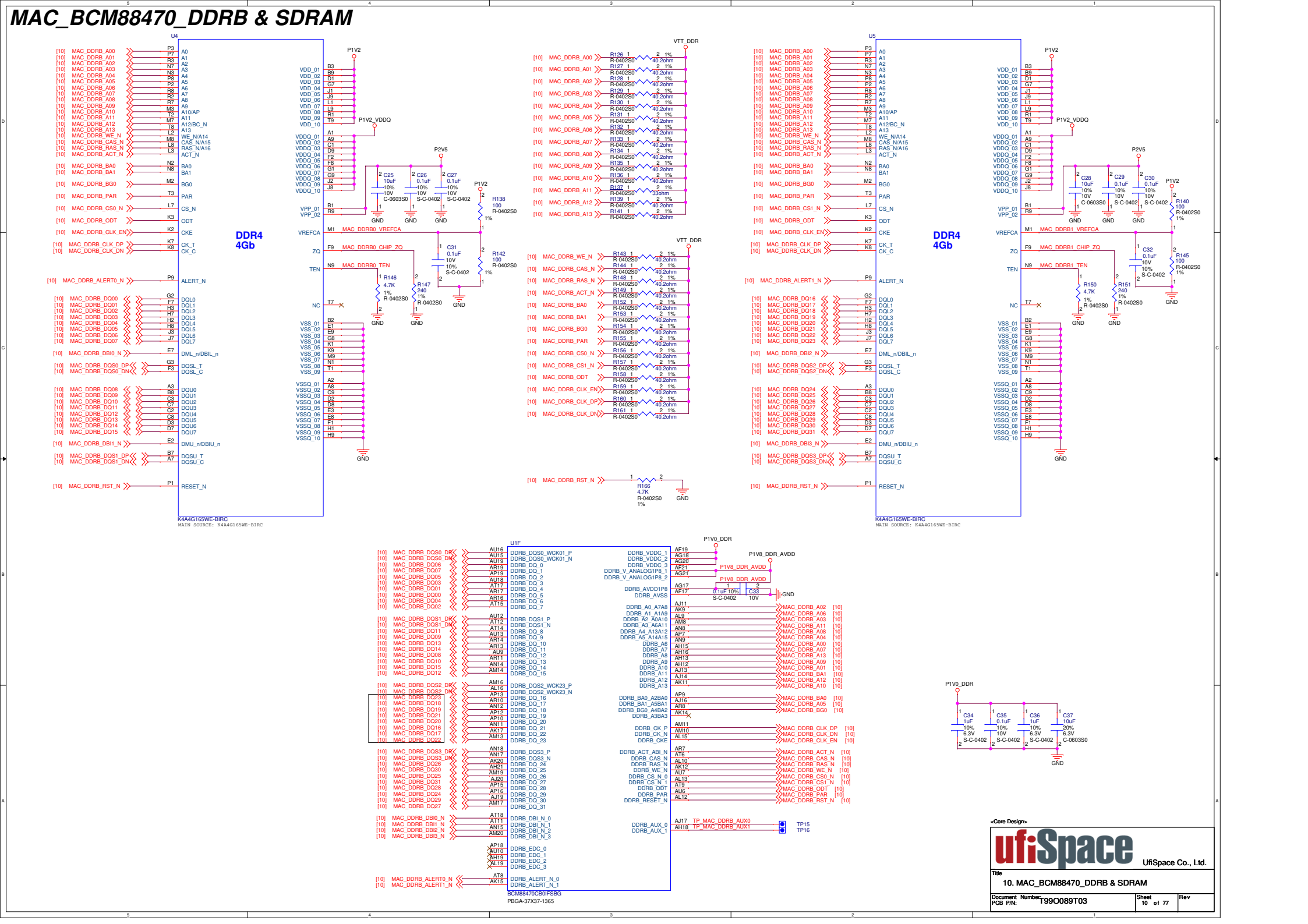


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UfiSpace Co., Ltd.

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09. MAC_BCM88470_DDRA & SDRAM

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MAC_BCM88470_DDRB & SDRAM

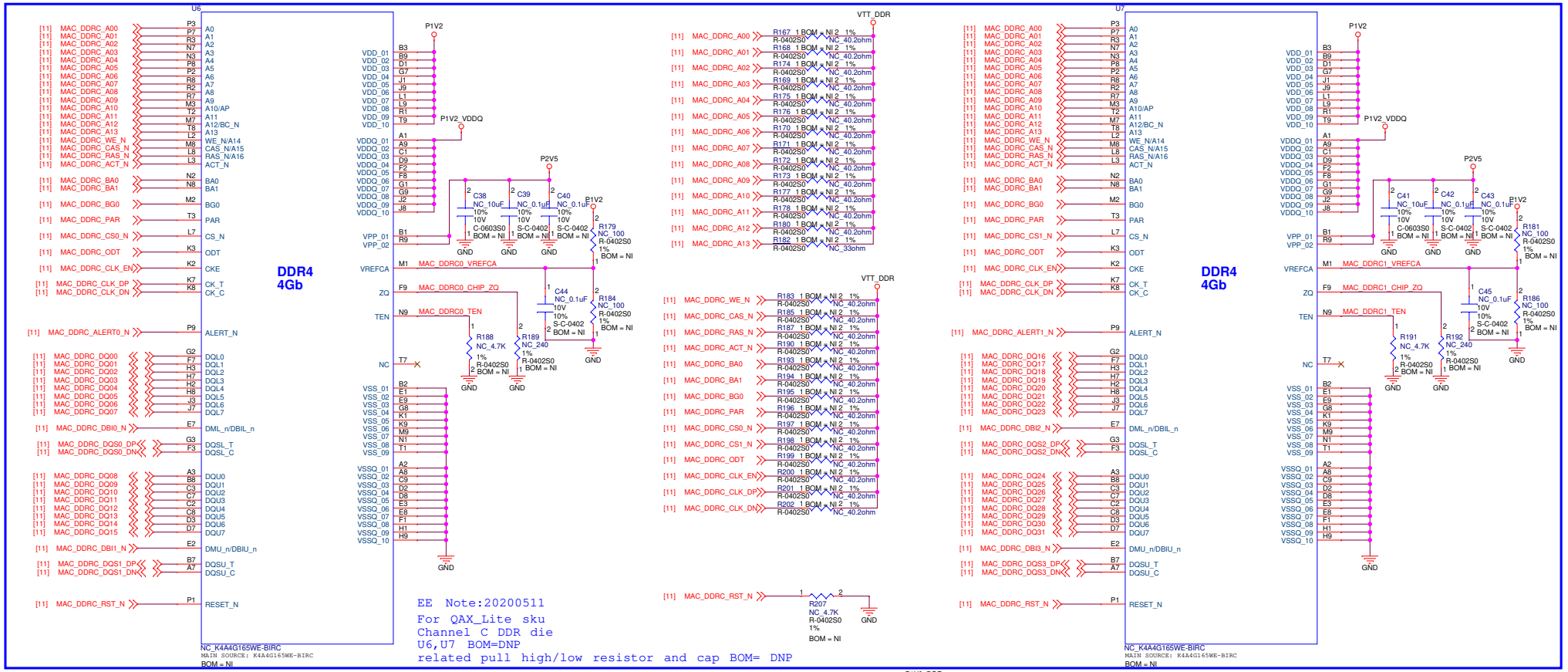


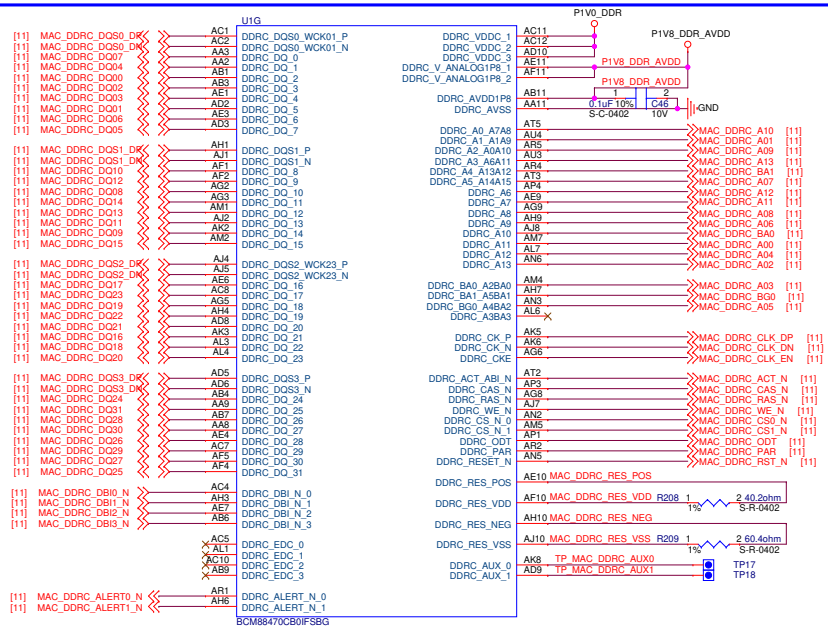
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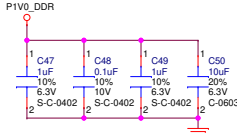
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10. MAC_BCM88470_DDRB & SDRAM

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MAC_BCM88470_DDRC & SDRAM







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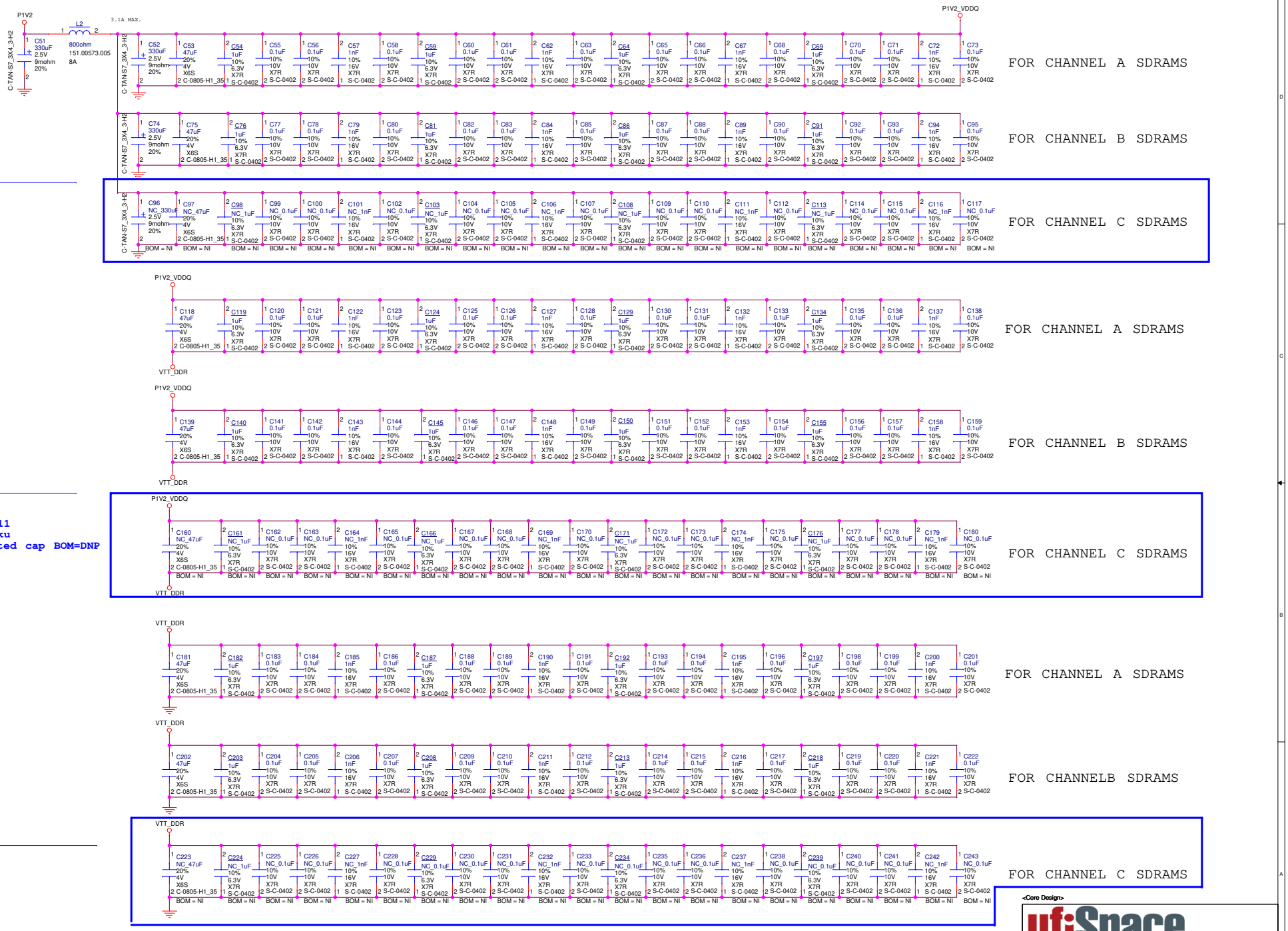
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Title

11. MAC_BCM88470_DDRC & SDRAM

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MAC_BCM88470_DDR_DECAPS1



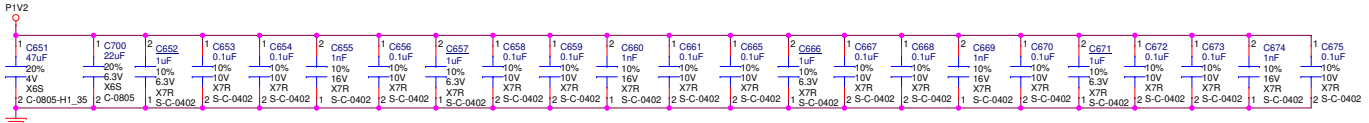
EE Note:20200511
For QAX_Lite Sku
Channel C related cap BOM=DNP

<Core Design>
UfiSpace Co., Ltd.

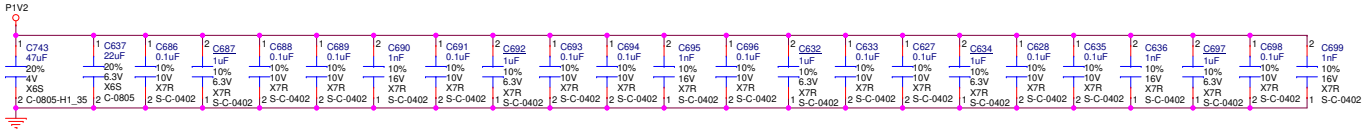
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12. MAC_BCM88470_DDR_DECAPS1

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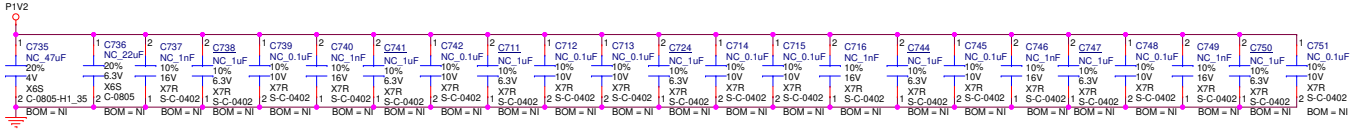
MAC_BCM88470_DDR_DECAPS2



FOR CHANNEL A SDRAMS



FOR CHANNELB SDRAMS



FOR CHANNEL C SDRAMS

EE Note:20200511
For QAX_Lite Sku
Channel C related cap BOM=DNP

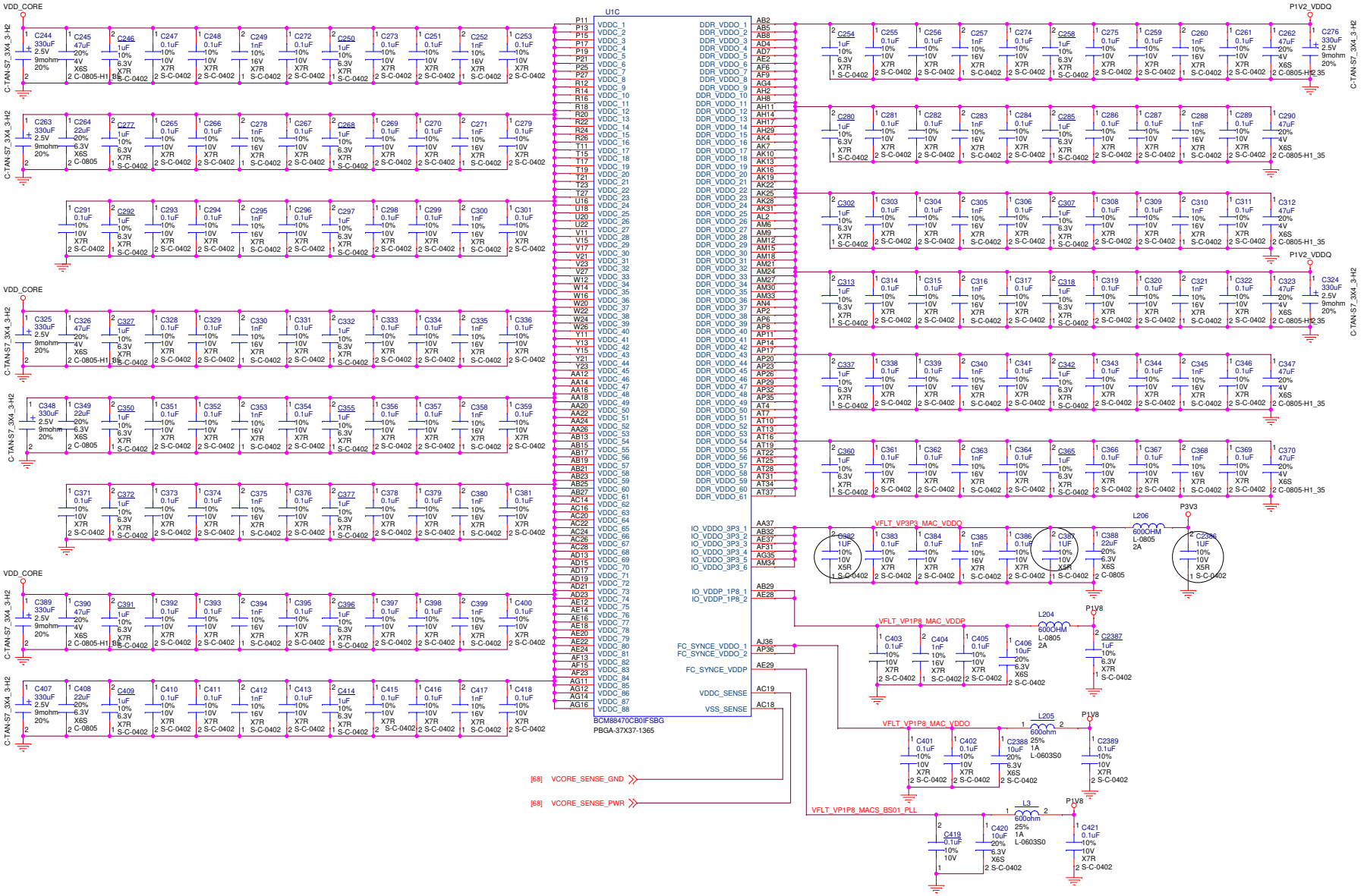
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Title: 13. MAC_BCM88470_DDR_DECAPS2

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MAC_BCM88470_PWR1



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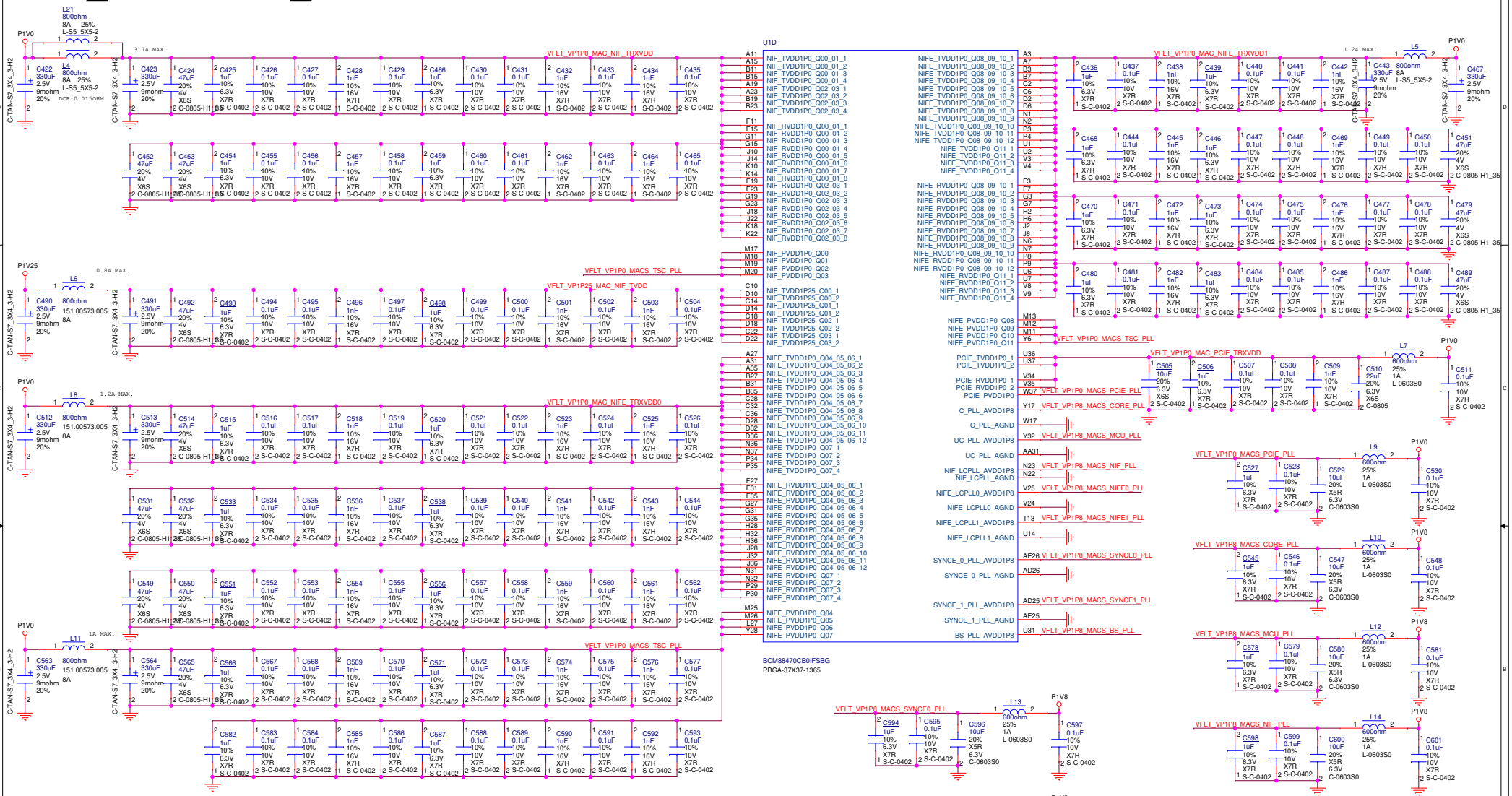
UfiSpace Co., Ltd.

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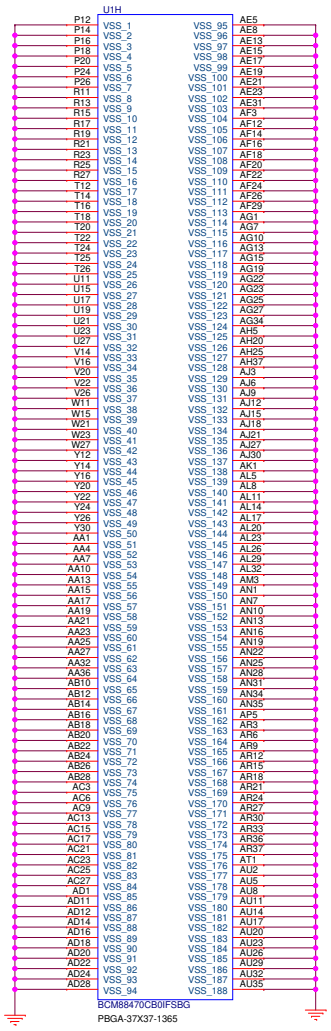
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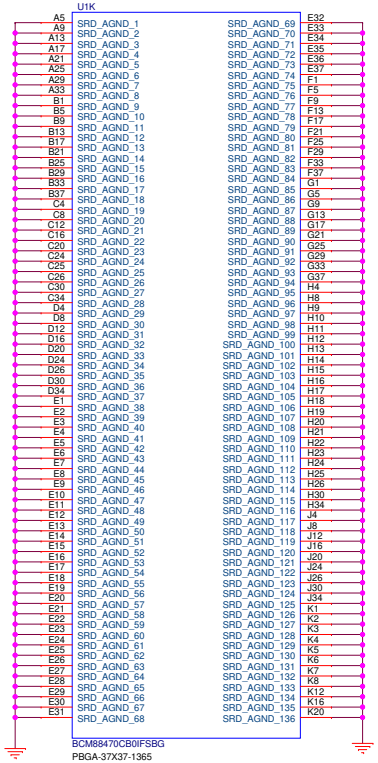
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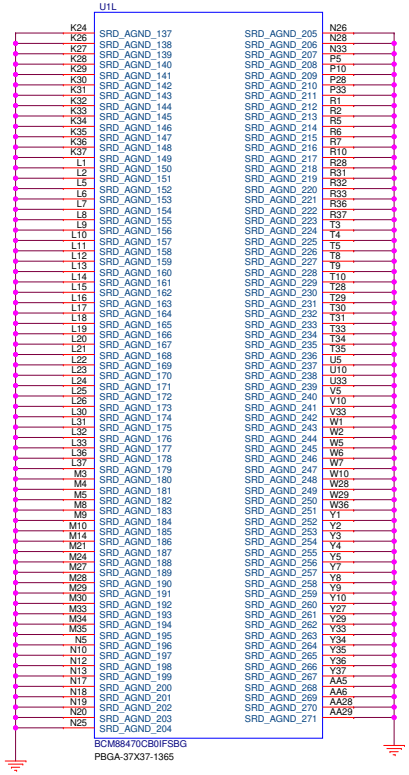
MAC_BCM88470_PWR2



MAC_BCM88470_GND







<Core Design>

UfiSpace Co., Ltd.

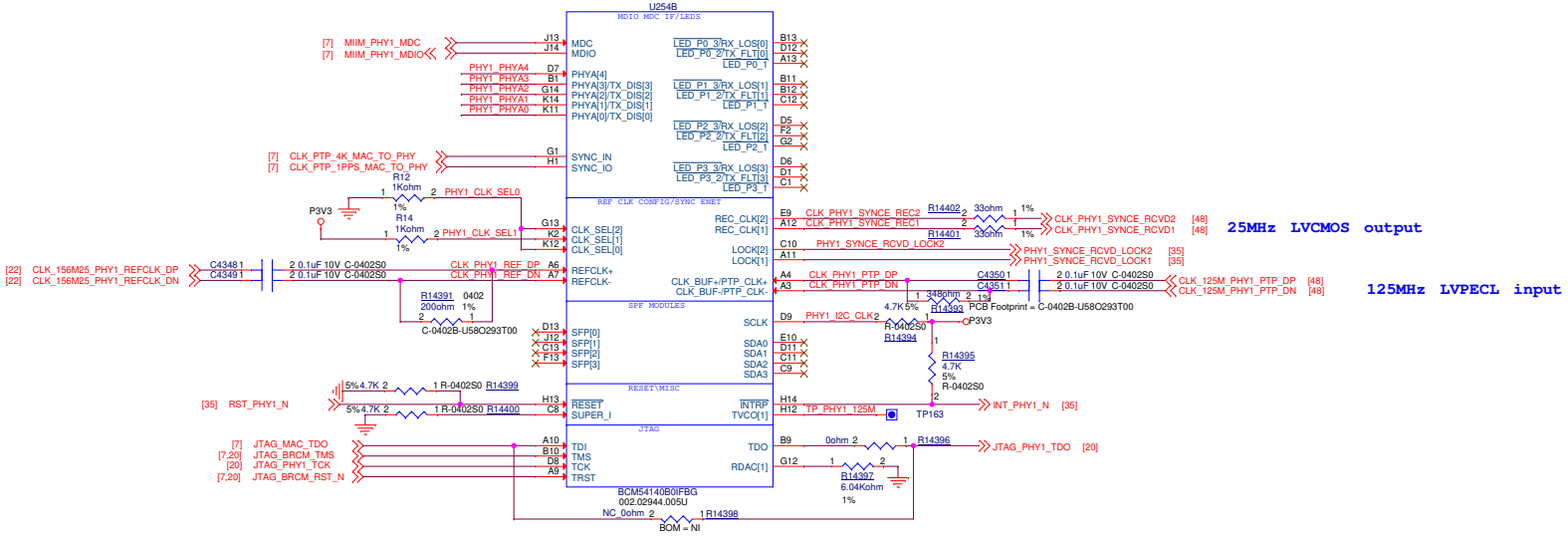
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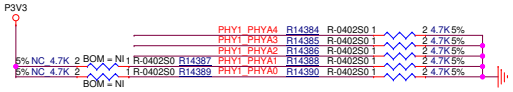
16. MAC_BCM88470_GND

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PHY1_BCM54140_CLOCK & MISC

		PHY 1
ADDR SETTING	ADDR_0	0
	ADDR_1	0
	ADDR_2	0
	ADDR_3	0
	ADDR_4	0
PHY ADDR	Port 0	00000
	Port 1	00001
	Port 2	00010
	Port 3	00011





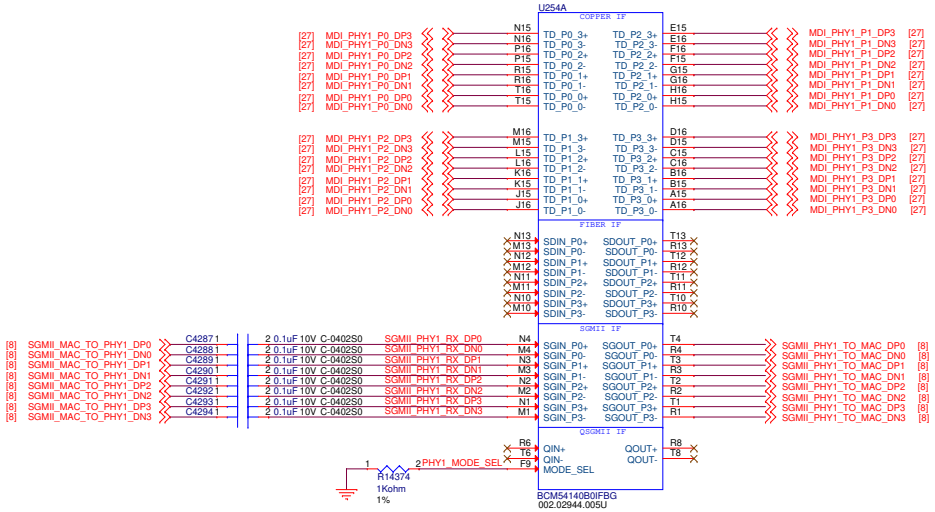
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Title: 17. PHY1_BCM54140_CLOCK & MISC

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PHY1_BCM54140_MDI & SERDES



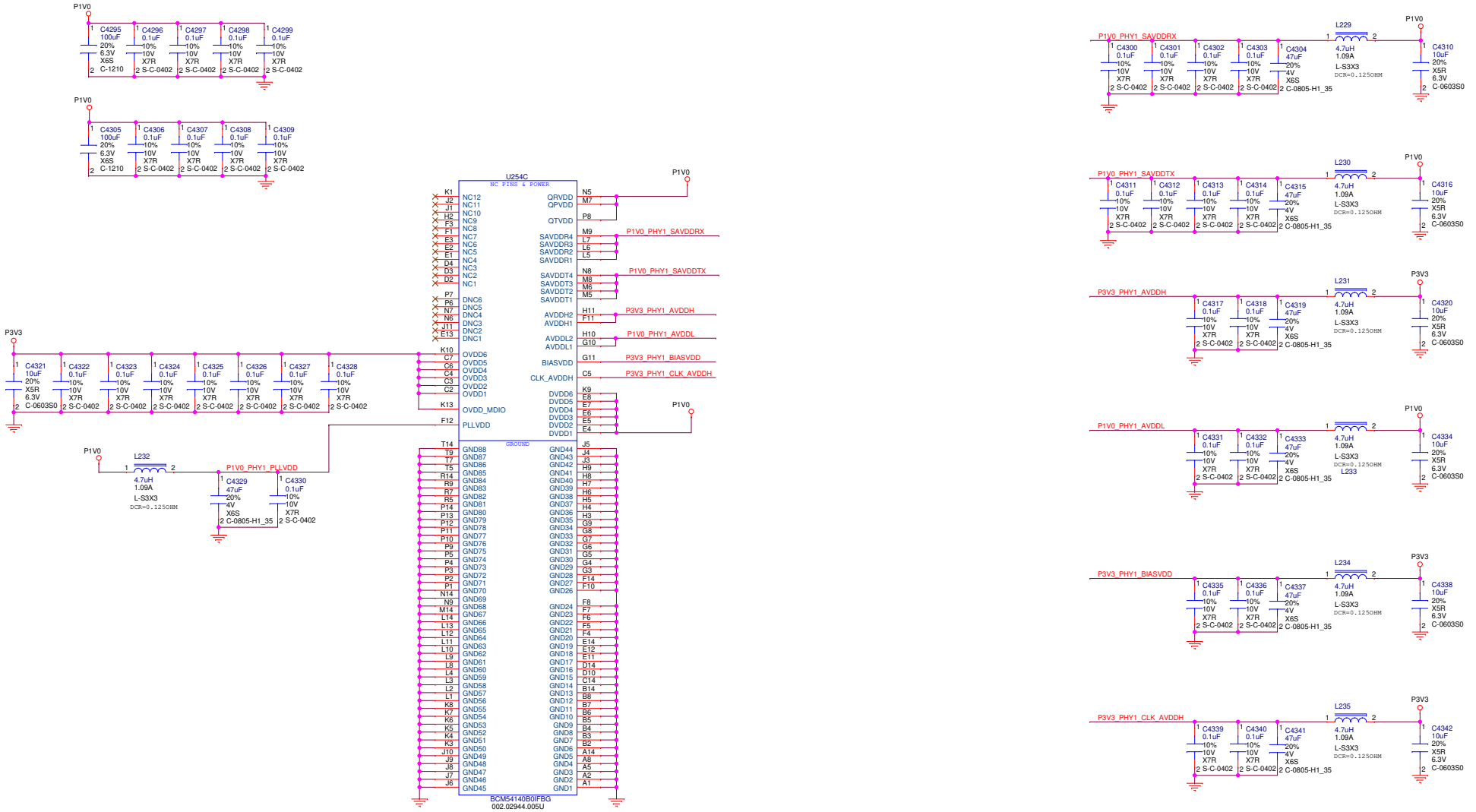
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Title: 18. PHY1_BCM54140_MDI & SERDES

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PHY1_BCM54140_PWR & GND



<Core Design>

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Title: 19. PHY1_BCM54140_PWR & GND

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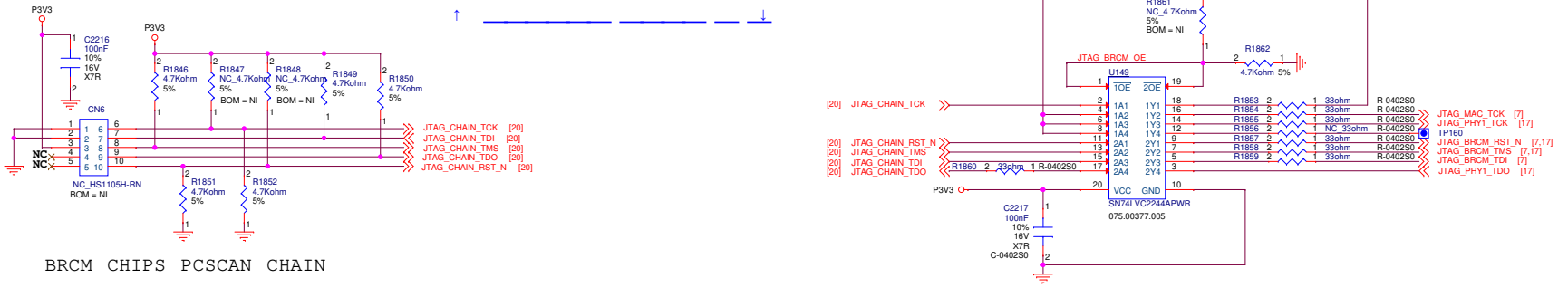
PCB P/N:

JTAG CHAIN & TSPLL CLOCK

JTAG CHAIN

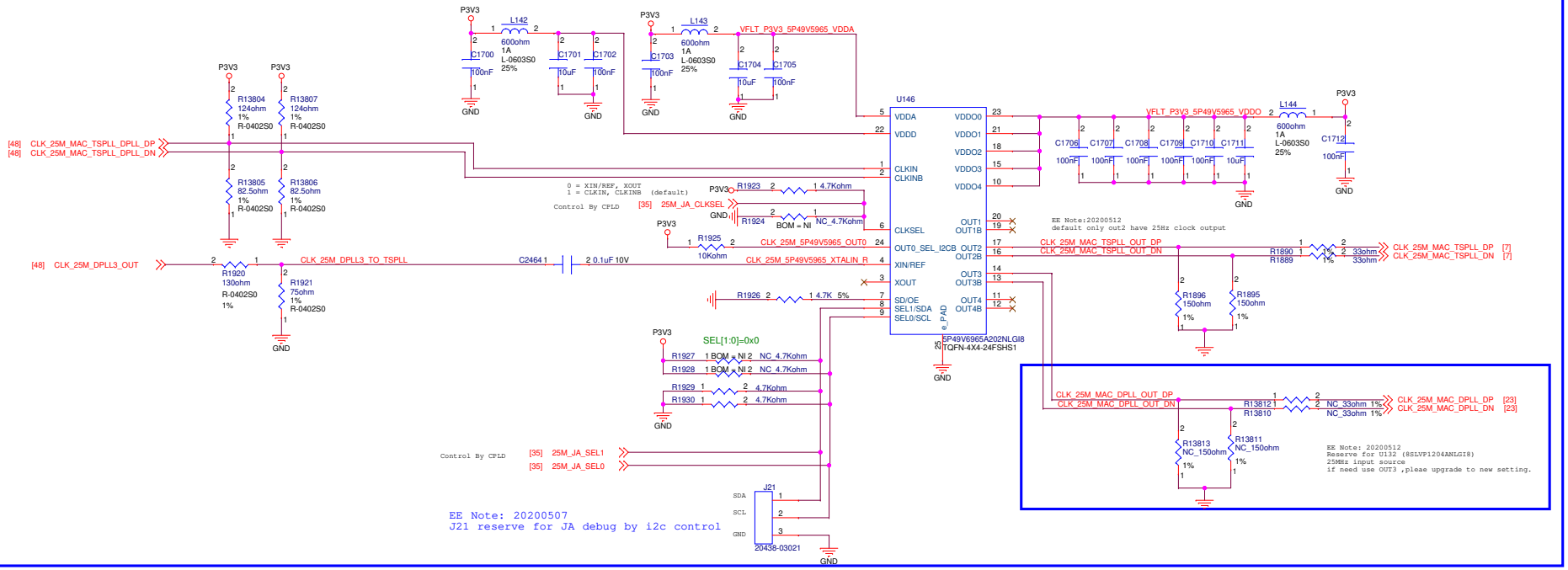
SAID Jtag Chain
CN6-->U149-->U1_BCM88470-->U25_BCM82398-->U23_BCM82780

Q-AX Lite Jtag Chain
CN6-->U149-->U1_BCM88470-->U254_BCM54140



BRCM CHIPS PCSCAN CHAIN

TSPLL_25MHz CLOCK



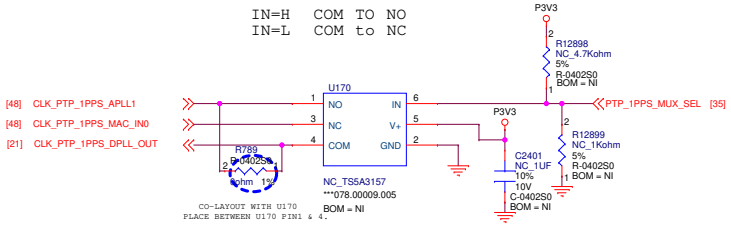
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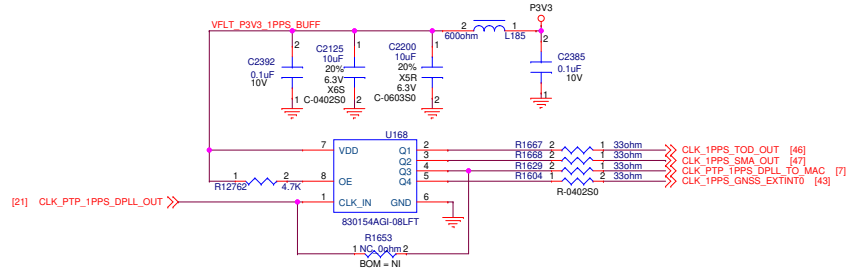
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Title: 20. JTAG CHAIN & TSPLL CLOCK

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PCB P/N:

CLOCK BUFFER1_1PPS & 4K





EE Note:20200602
For QAX_Lite sku
remove PTP_CLK Buffer and connect CLK_PTP_4K from MAC to PHY directly
remove 1PPS_CLK Buffer and connect 1PPS_CLK from MAC to PHY directly

<Core Design>

UfiSpace Co., Ltd.

Title: 21. CLOCK BUFFER1_1PPS & 4K

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CLOCK BUFFER2_156.25M

EE Note:20200602
remove
Si5344D IN0 input

CML

EE Note:20200602
remove
Si5344D IN1 input

LVPECL

[48] CLK_156M25_PTP_REF_DP — C2366 1 — 2 0.1uF 10V C-0402S0 — CLK_156M25_DPLL_REFCLK_DP [22]
[48] CLK_156M25_PTP_REF_DN — C2367 1 — 2 0.1uF 10V C-0402S0 — R12482 1% 100ohm — CLK_156M25_DPLL_REFCLK_DN [22]

IN_SEL[1:0]		Selected Input
0	0	IN0
0	1	IN1
* 1	0	IN2

IN_SEL[1:0] : Internal pulled up

An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode.
NEED CHANGE TO 48MHZ
2016 SIZE XTAL.

Y1 48MHz O-S2X1_6-4DS0
XTAL_SHIELD
CLKGEN_54M_XTAL_IN
CLKGEN_54M_XTAL_OUT
XTAL_SHIELD

EE Note:20200602
remove
Si5344D IN0 input
EE Note:20200602
remove
Si5344D IN1 input

U135 Si5344D

FROM DPLL
[22] CLK_156M25_DPLL_REFCLK_DP
[22] CLK_156M25_DPLL_REFCLK_DN

INPUT SELECT: IN2
IN_SEL1
IN_SEL0

[35] INT_CJA_LOL_N
[22,35] INT_CJA_INTR_N
TP95
[42,48] I2C_CLK_SDA — 0ohm R1897
[42,48] I2C_CLK_SCL — 0ohm R1898
[22] JITTER_A1
[22] JITTER_A0
Si5344B_OE_N — BOM = NI R1980 NC_4.7Kohm
[35] RST_CJA_N

Si5344D-D09606-GMR
031.00535.005U

/OE : Internal pulled low
/RST : Internal pulled up

RST pin is internally pulled up with a ~20 kΩ resistor to the voltage selected by the IO_VDD_SEL bit

VFLT_P3V3_JA_VDDO
VFLT_P1V8_JA_VDD
VFLT_P3V3_JA_VDDA
VFLT_P3V3_JA_VDDS

Close to MAC BCM88470

OUT0 CLK_156M25_OUT0_NIF_LCPLL_DP — R13072 33ohm — C2167 — CLK_156M25_MAC_NIF_LCPLL_DP [7]
OUT0 CLK_156M25_OUT0_NIF_LCPLL_DN — R13073 33ohm — C2168 — CLK_156M25_MAC_NIF_LCPLL_DN [7] — LVPECL
OUT1 CLK_156M25_OUT1_NIFE_LCPLL0_DP — R13074 33ohm — C2165 — CLK_156M25_MAC_NIFE_LCPLL0_DP [7]
OUT1 CLK_156M25_OUT1_NIFE_LCPLL0_DN — R13075 33ohm — C2166 — CLK_156M25_MAC_NIFE_LCPLL0_DN [7] — LVPECL
OUT2 CLK_156M25_OUT2_NIFE_LCPLL1_DP — R13076 33ohm — C2163 — CLK_156M25_MAC_NIFE_LCPLL1_DP [7]
OUT2 CLK_156M25_OUT2_NIFE_LCPLL1_DN — R13077 33ohm — C2164 — CLK_156M25_MAC_NIFE_LCPLL1_DN [7] — LVPECL
OUT3 CLK_156M25_OUT3_REF0_DP — 33ohm R12751 — CLK_156M25_PHY1_REFCLK_DP [17]
OUT3 CLK_156M25_OUT3_REF0_DN — 33ohm R12750 — CLK_156M25_PHY1_REFCLK_DN [17] — LVPECL — To PHY1

EE Note:20200602
For QAX_Lite sku
modify out3 clock to CLK_156M25_PHY1_REFCLK_DN/DP

I2C address: 11010 A1 A0 ; 0x6B

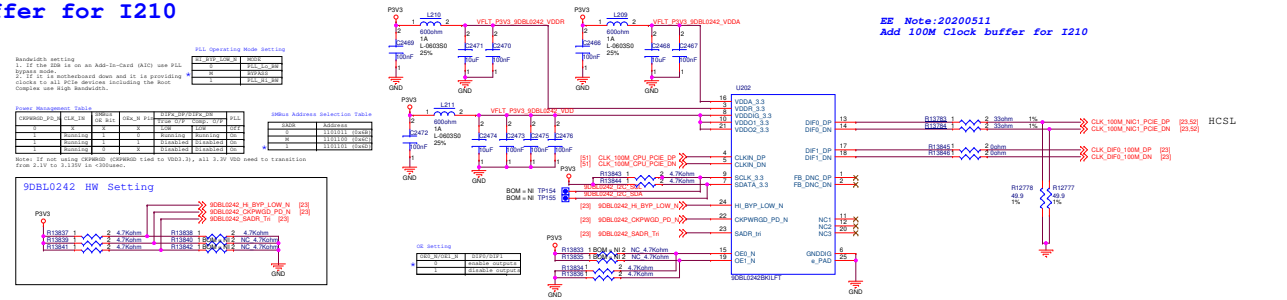
JITTER_A1 [22]
JITTER_A0 [22]

EE Note:20200602
remove 156.25MHz_CLK Buffer to PHY1/PHY3 and related circuit

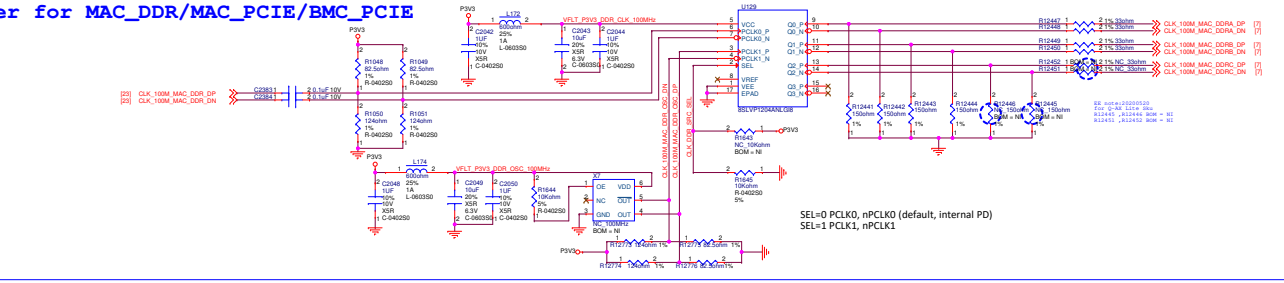
<Core Design>
UfiSpace Co., Ltd.
Title: 22. CLOCK BUFFER2_156.25M
Document Number: T99O089T03
PCB P/N:
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Rev

CLOCK BUFFER3_25M & 100M

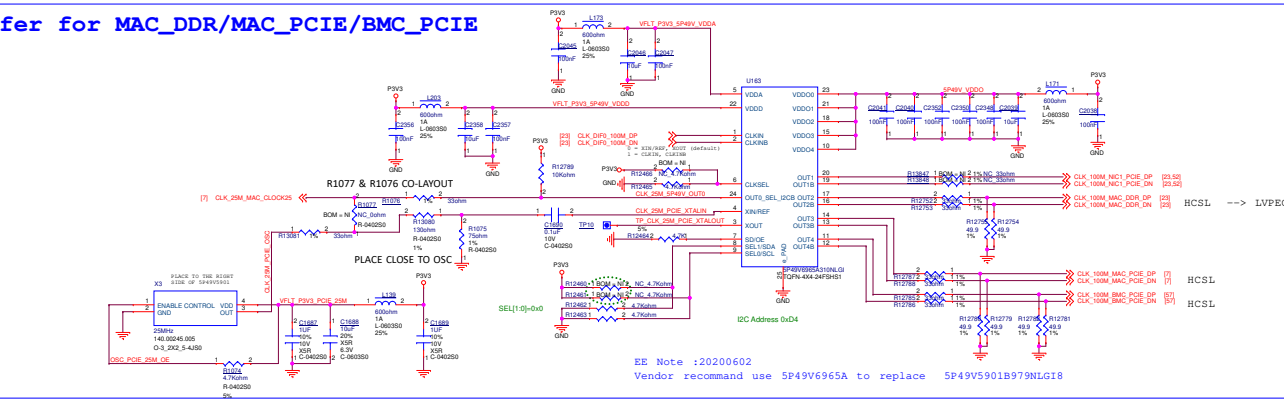
100MHz Clock Buffer for I210



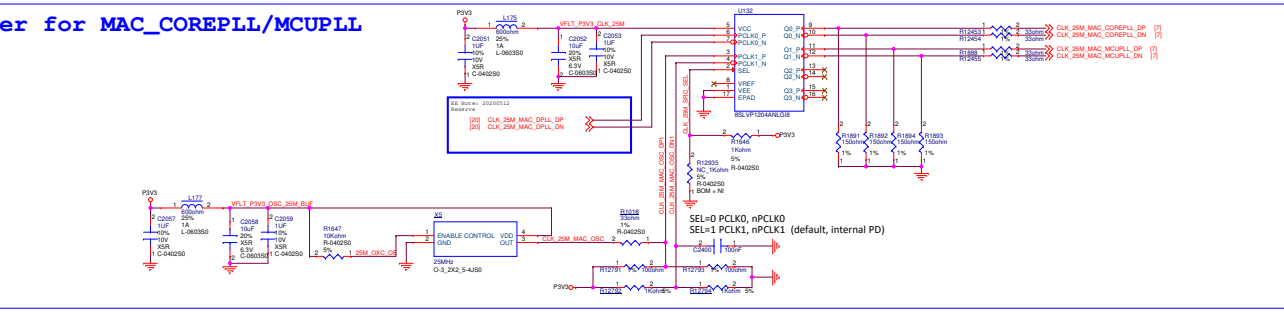
100MHz Clock Buffer for MAC_DDR/MAC_PCIE/BMC_PCIE



100MHz Clock Buffer for MAC_DDR/MAC_PCIE/BMC_PCIE



25MHz Clock Buffer for MAC_COREPLL/MCUPLL



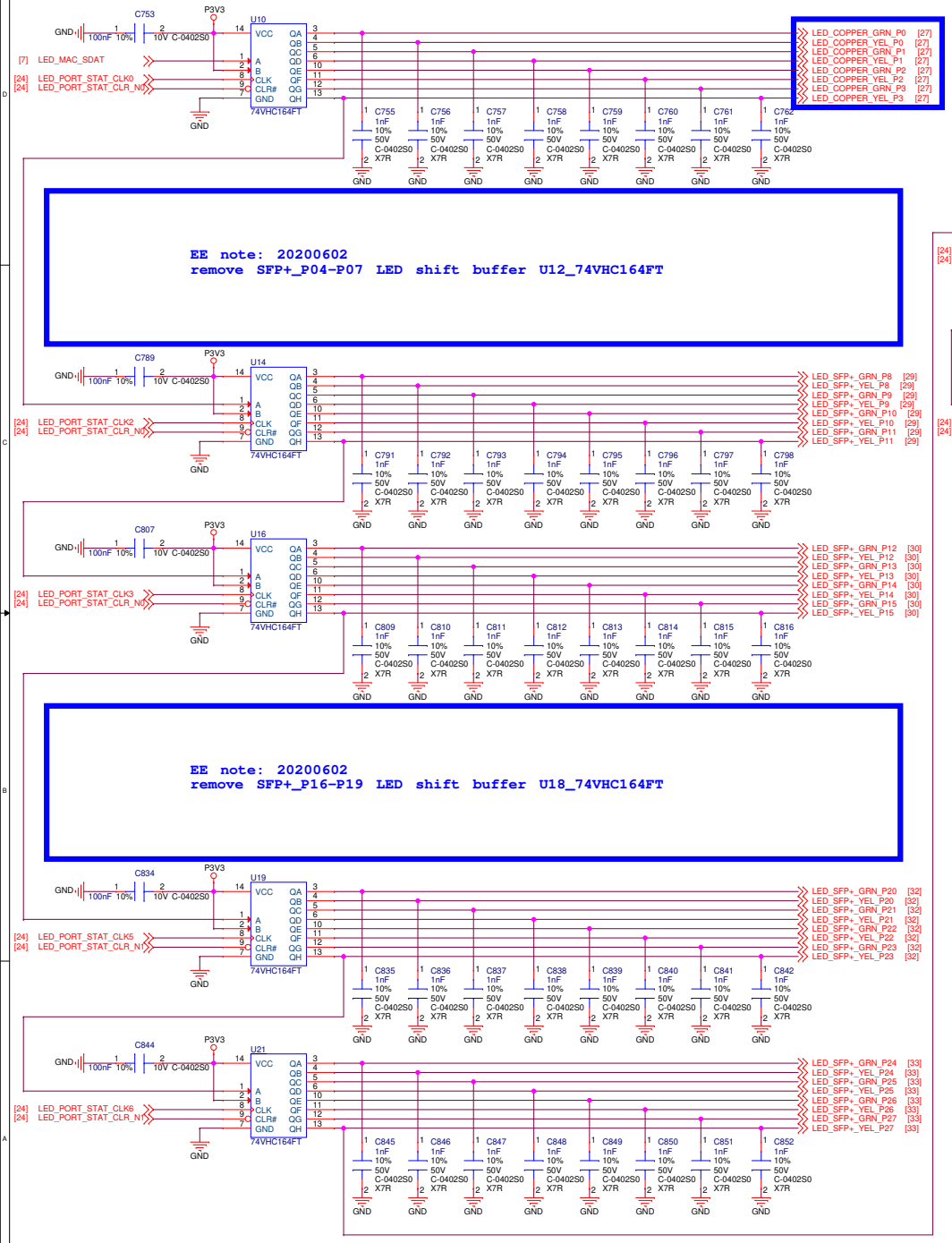
<Core Design>

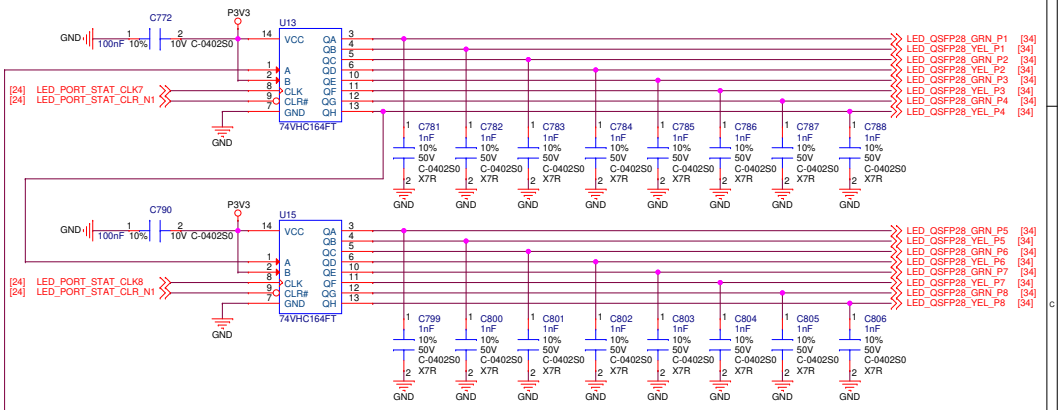
ufiSpace

UfiSpace Co., Ltd.

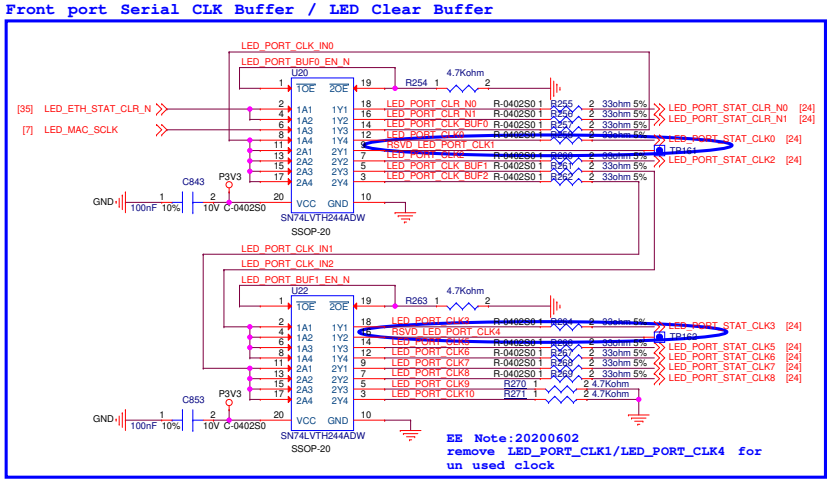
Title	23. CLOCK BUFFER3_25M & 100M
Document Number: PCB P/N:	T99O089T03
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PORT STATUS LED CONTROL





Front port Serial CLK Buffer / LED Clear Buffer



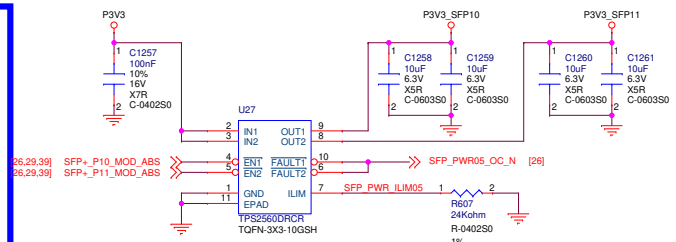
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UfiSpace Co., Ltd.

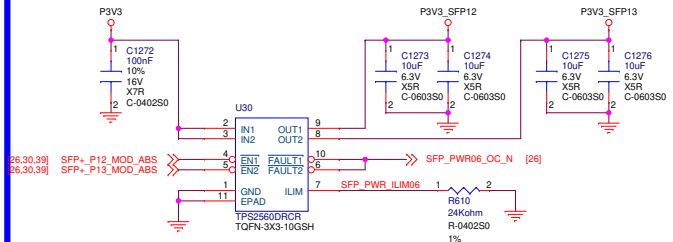
Title: 24. PORT STATUS LED CONTROL

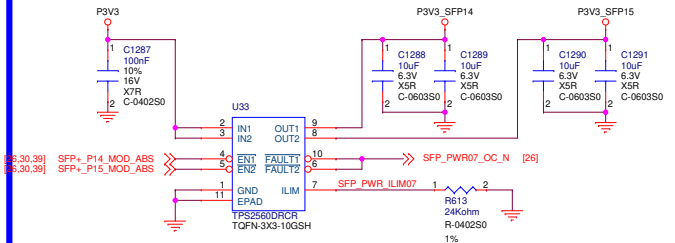
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FIBER PORTS PWR SWITCH1

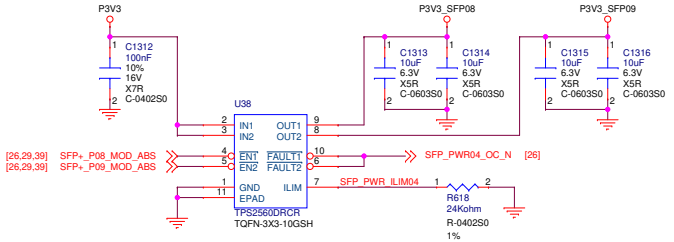
EE Note:20200602
remove
SFP+_P00-P07 Current Limiter

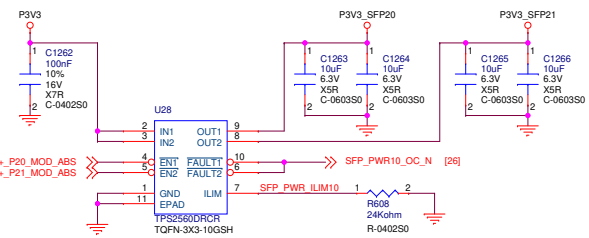


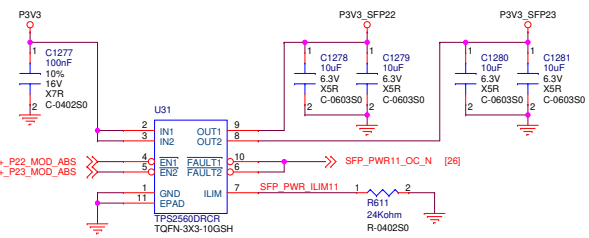


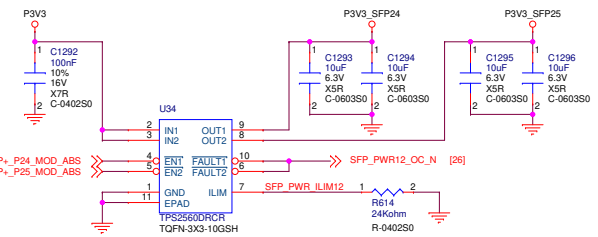


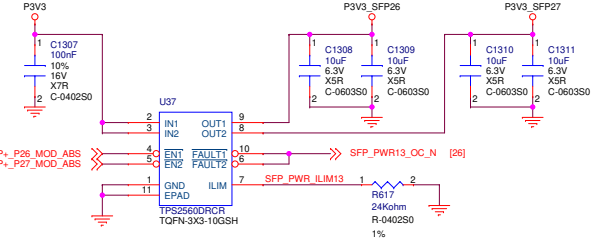
EE Note:20200602
remove
SFP+_P16-P19 Current Limiter











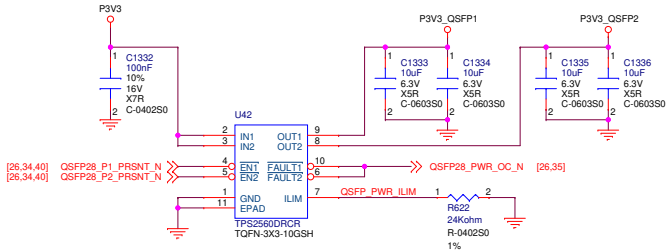
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UfiSpace Co., Ltd.

Title
25. FIBER PORTS PWR SWITCH1

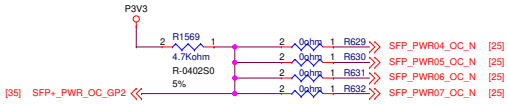
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FIBER PORTS PWR SWITCH2

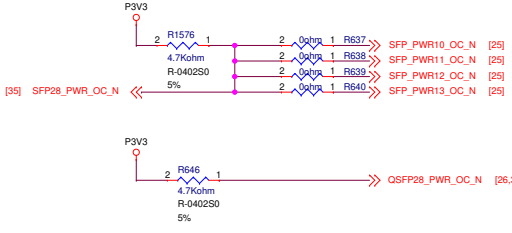


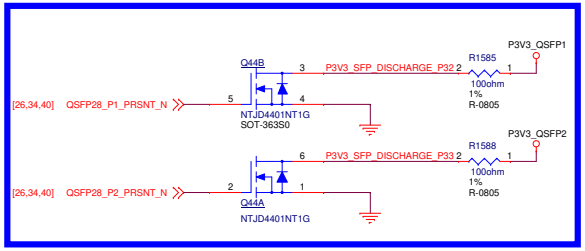
EE Note:202020602
Add back
QSFP28_P1-P2 Current Limiter

EE Note:202020506
remove
SFP+_PWR00-PWR07_OC related circuit



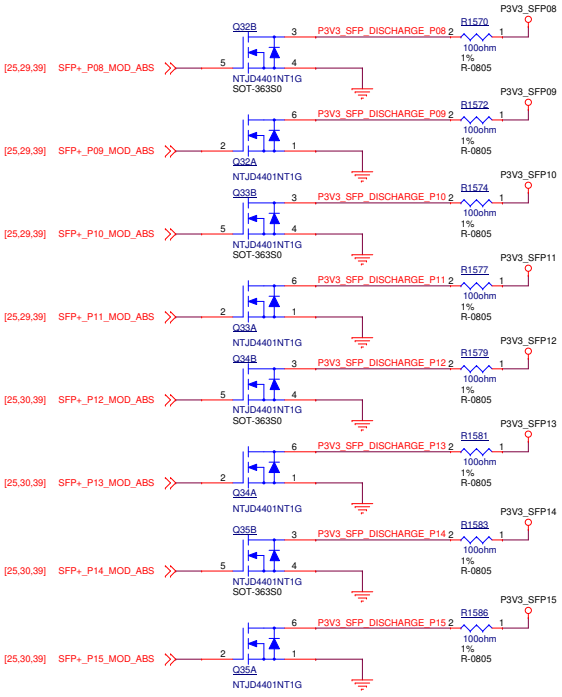
EE Note:202020602
remove
SFP+_PWR16-PWR19_OC related circuit





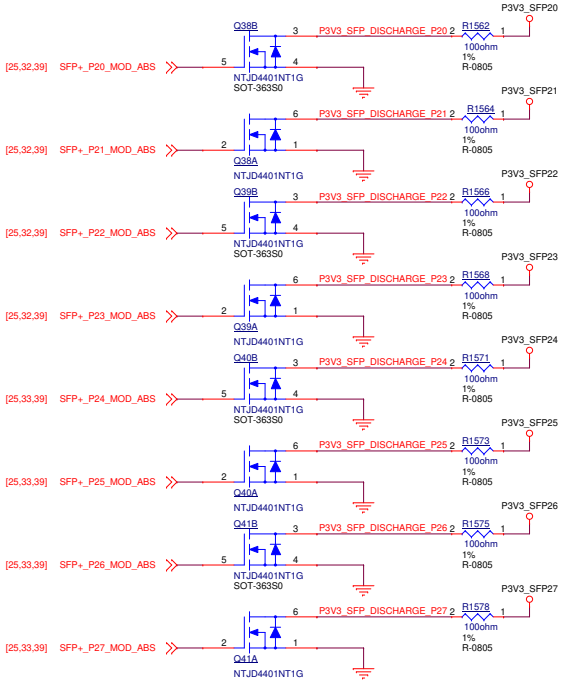
EE Note:20200602
add back
QSFP28_P1-P2 PRSNT related circuit

EE Note:202000602
remove
SFP+_P0-P7 ABS related circuit



NTJD4401NT1G RDS=0.92V

EE Note:202000602
remove
SFP+_P16-P19 ABS related circuit



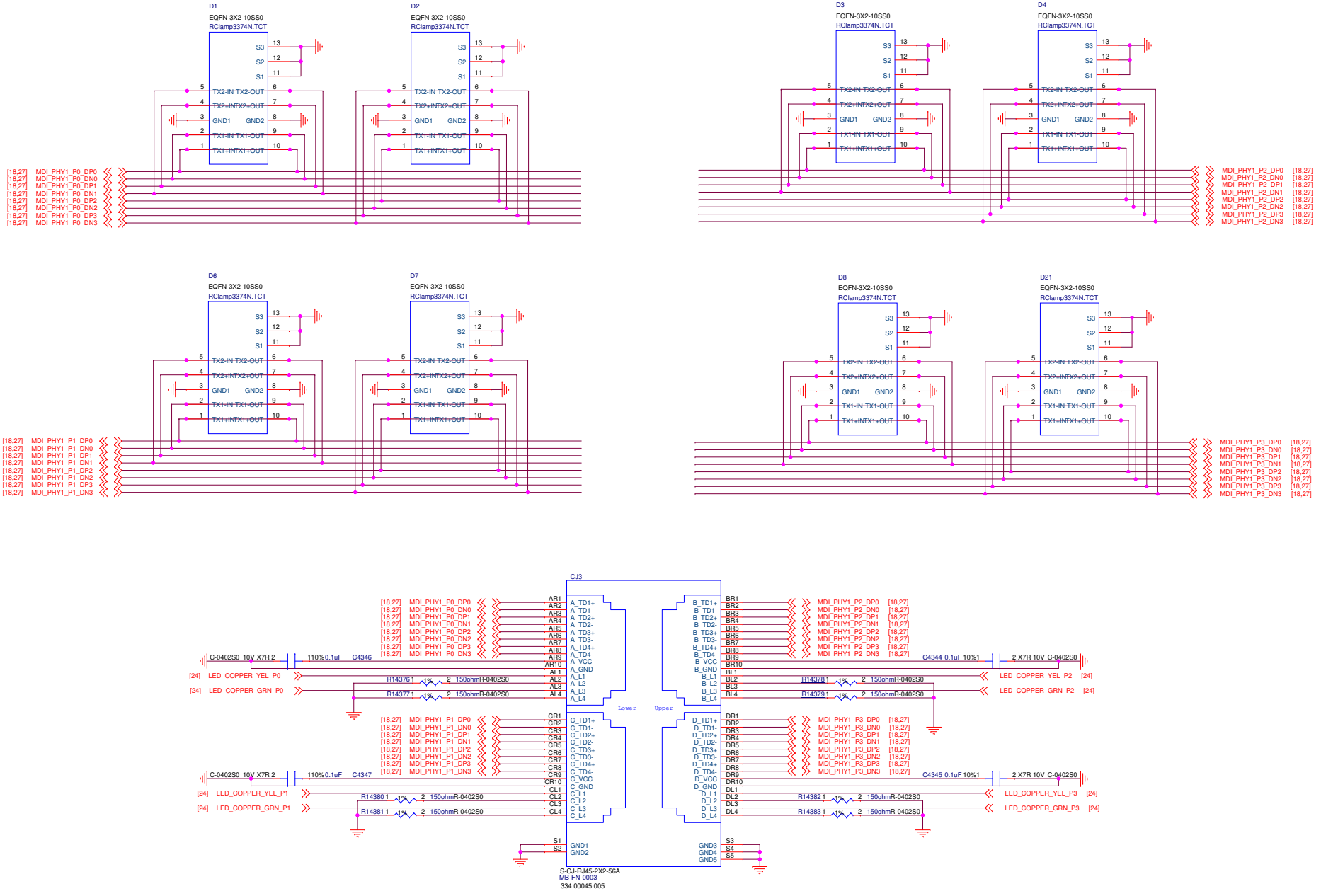
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Title
26. FIBER PORTS PWR SWITCH2

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2x2 ICM_CONN_P00~P03



Q-AX Lite

0	2
1	3

4	6	8	10
5	7	9	11

12	14	16	18
13	15	17	19

Z1
Z2

<Core Design>

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Title

27. 2x2 ICM_CONN_P00~P03

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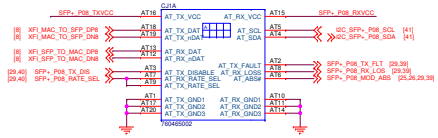
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Document Number: PCB P/N: T99O089T03	Sheet 28 of 77	Rev

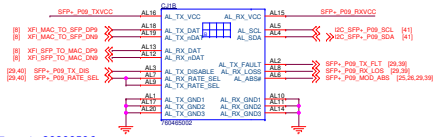
2x4 SFP+_CONN1_P04~P07

2x4 SFP+_CONN1_P04



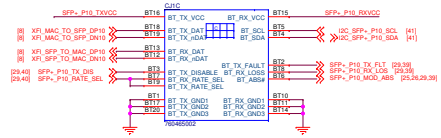
EE note20200506
change to 2x4_SFP+ Cage

2x4 SFP+_CONN1_P05



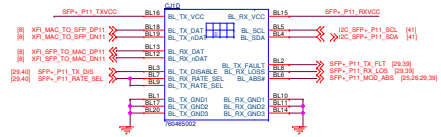
EE note20200506
change to 2x4_SFP+ Cage

2x4 SFP+_CONN1_P06



EE note20200506
change to 2x4_SFP+ Cage

2x4 SFP+_CONN1_P07



EE note20200506
change to 2x4_SFP+ Cage

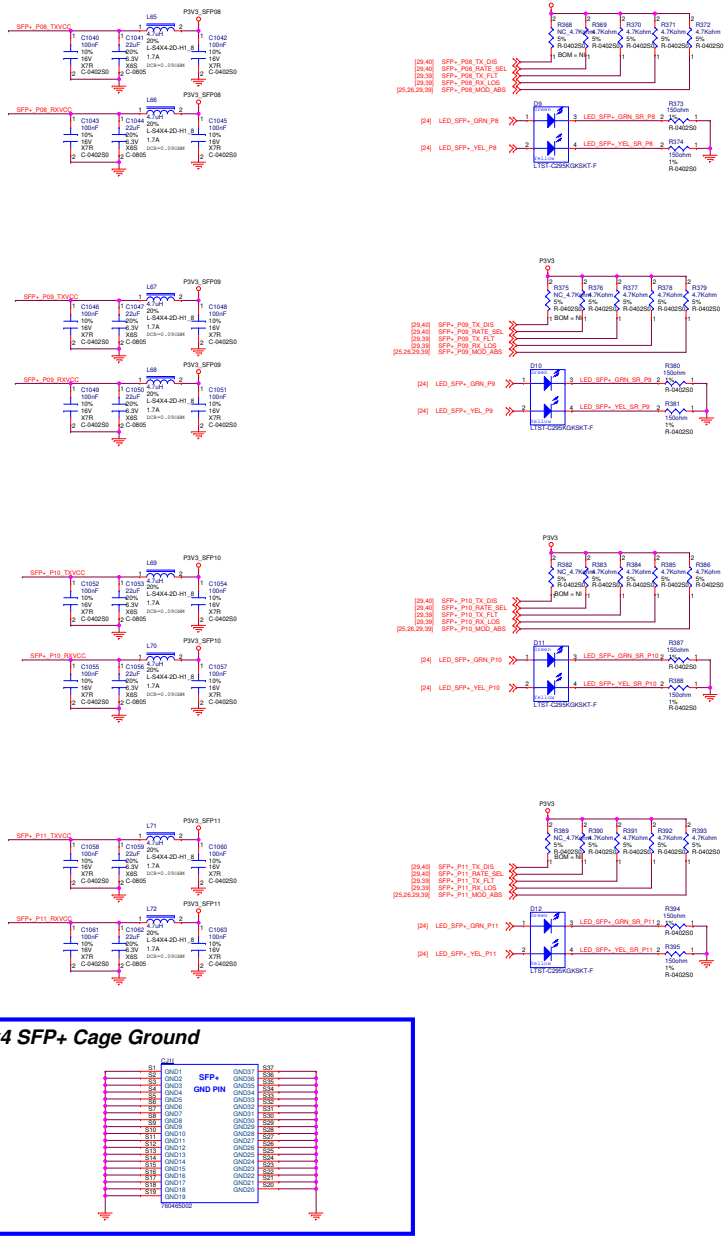
Q-AX Lite

0	2
1	3

4	6	8	10
5	7	9	11

12	14	16	18
13	15	17	19

Z1
Z2



2x4 SFP+ Cage Ground

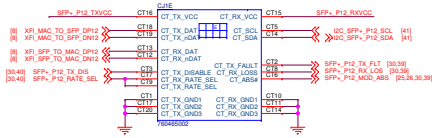
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ufiSpace
UfiSpace Co., Ltd.

Title: 29. 2x4 SFP+_CONN1_P04~P07

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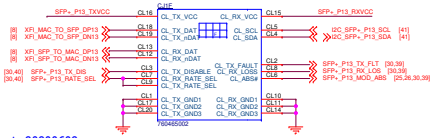
2x4 SFP+_CONN1_P08~P11

2x4 SFP+_CONN1_P08



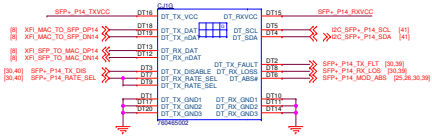
EE note20200602
change to 2x4 SFP+ Cage

2x4 SFP+_CONN1_P09



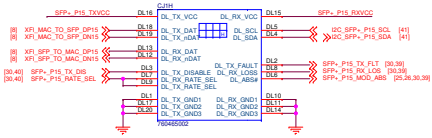
EE note20200602
change to 2x4 SFP+ Cage

2x4 SFP+_CONN1_P10



EE note20200602
change to 2x4 SFP+ Cage

2x4 SFP+_CONN1_P11



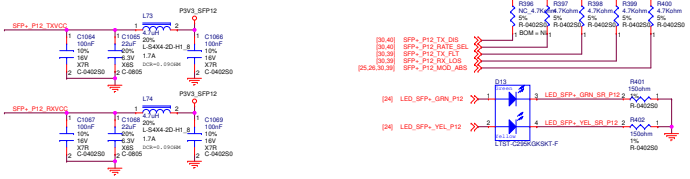
EE note20200602
change to 2x4 SFP+ Cage

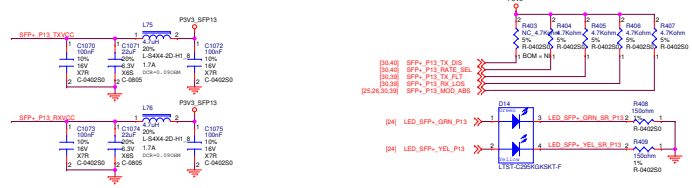
Q-AX Lite

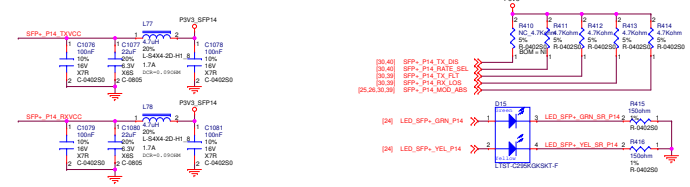
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1	3

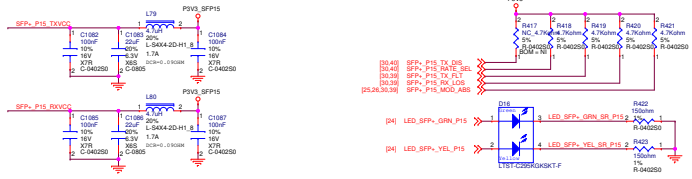
4	6	8	10
5	7	9	11

12	14	16	18	Z1
13	15	17	19	Z2









<Core Design>
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UfiSpace Co., Ltd.

Title	30. 2x4 SFP+_CONN1_P08~P11
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Title

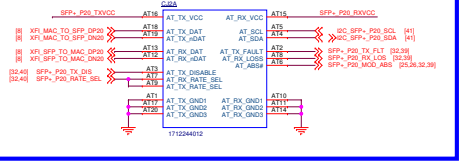
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Document Number: PCB P/N: T99O089T03	Sheet 31 of 77	Rev

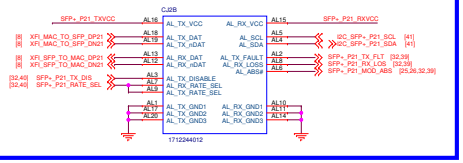
2x4 SFP28_CONN2_P12~P15

EE note20200602
change to 2x4 SFP28 Cage

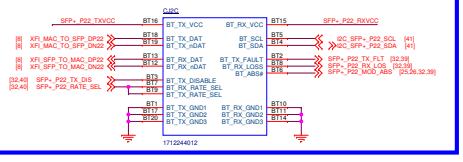
2x4 SFP28_CONN2_P12



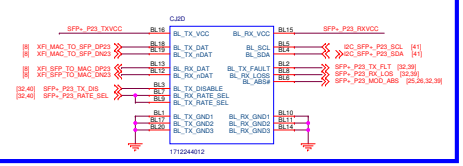
2x4 SFP28_CONN2_P13



2x4 SFP28_CONN2_P14



2x4 SFP28_CONN2_P15



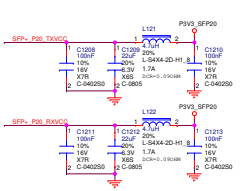
Q-AX Lite

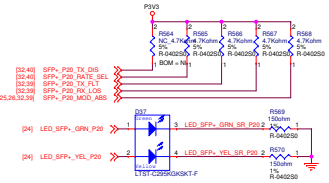
0	2
1	3

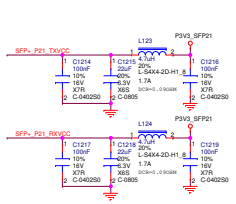
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5	7	9	11

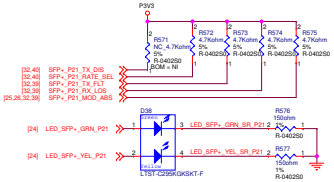
12	14	16	18
13	15	17	19

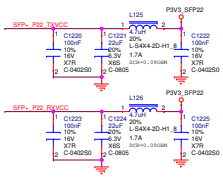
Z1
Z2

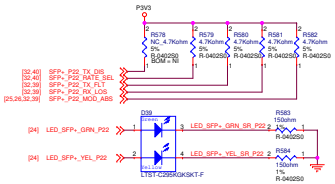


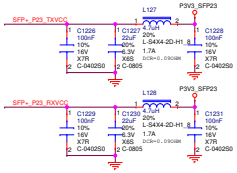


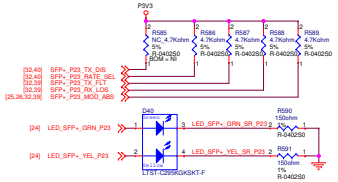




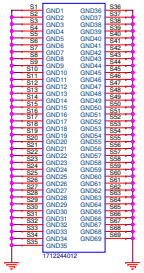








2x4 SFP28_Ground



<Core Design>

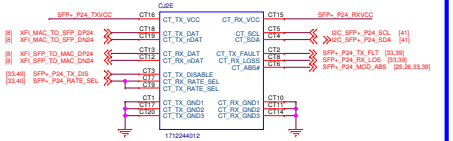
ufiSpace UfiSpace Co., Ltd.

Title	32. 2x4 SFP28_CONN2_P12~P15		
Document Number PCB P/N	T99O089T03	Sheet 32 of 77	Rev

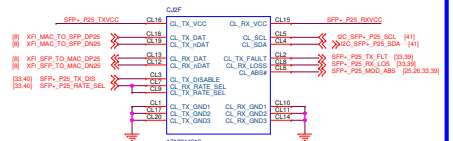
2x4 SFP28_CONN2_P16~P19

EE note20200504
Q-AX Lite 2x4 SFP28 Cage Silkscreen
co-layout with CSGR 2x8 SFP8 Cage

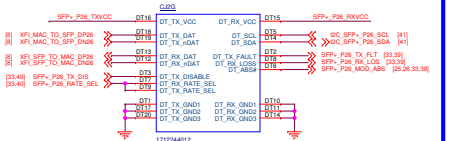
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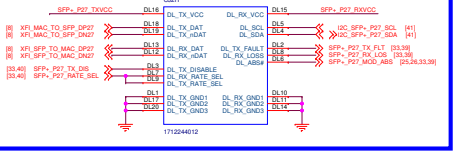
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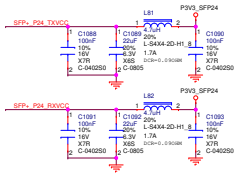


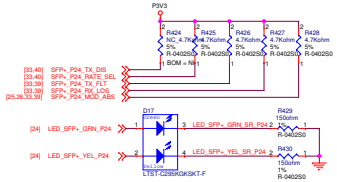
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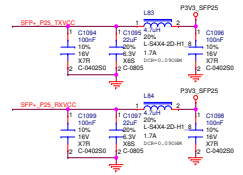


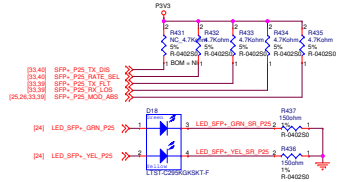
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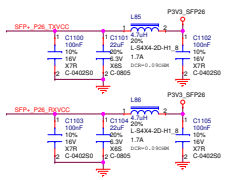


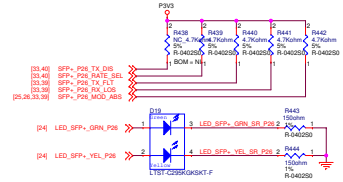


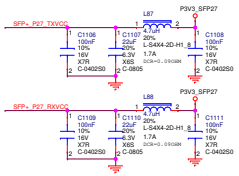


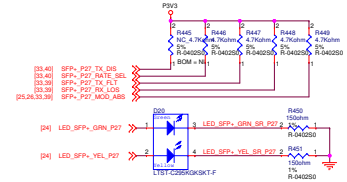












Q-AX Lite

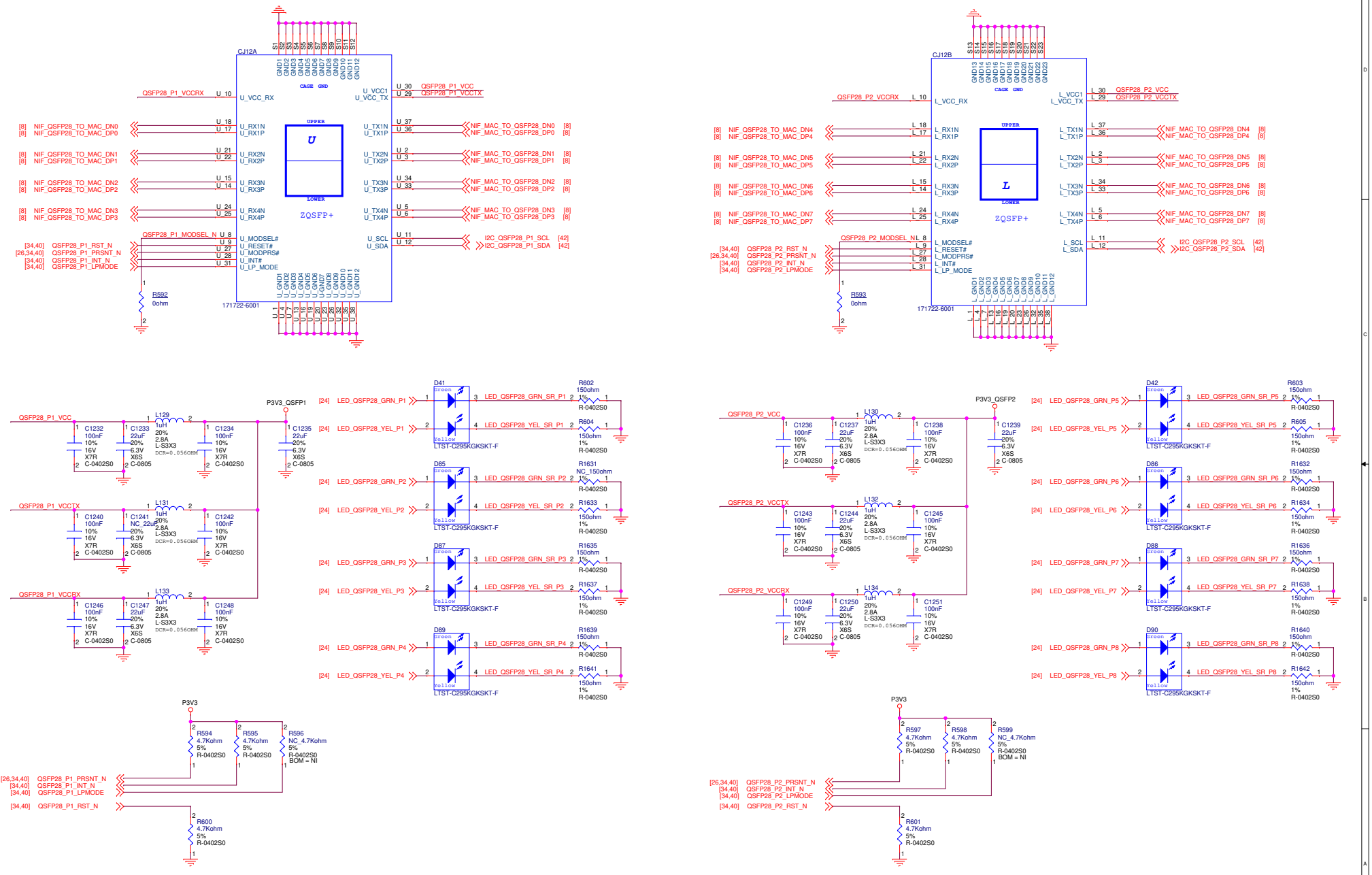
0	2
1	3

4	6	8	10
5	7	9	11

12	14	16	18
13	15	17	19

Z1
Z2

2x1 QSFP28 CONN3_Z01~Z02



Q-AX Lite

0	2
1	3

4	6	8	10
5	7	9	11

12	14	16	18
13	15	17	19

Z1
Z2

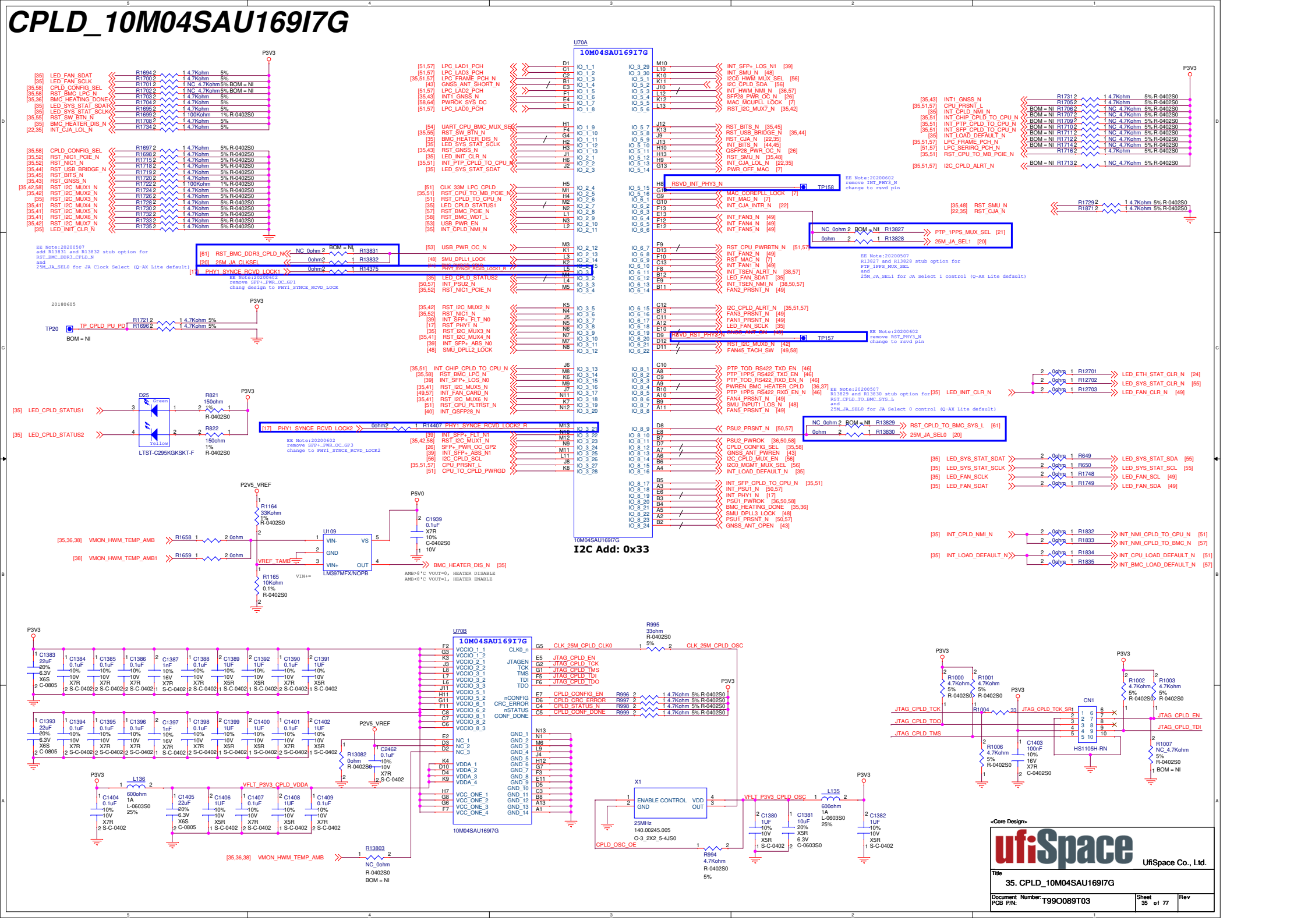
<Core Design>

UfiSpace Co., Ltd.

Title: 34. 2x1 QSFP28 CONN3_Z01~Z02

Document Number	Sheet	Rev
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CPLD_10M04SAU169I7G

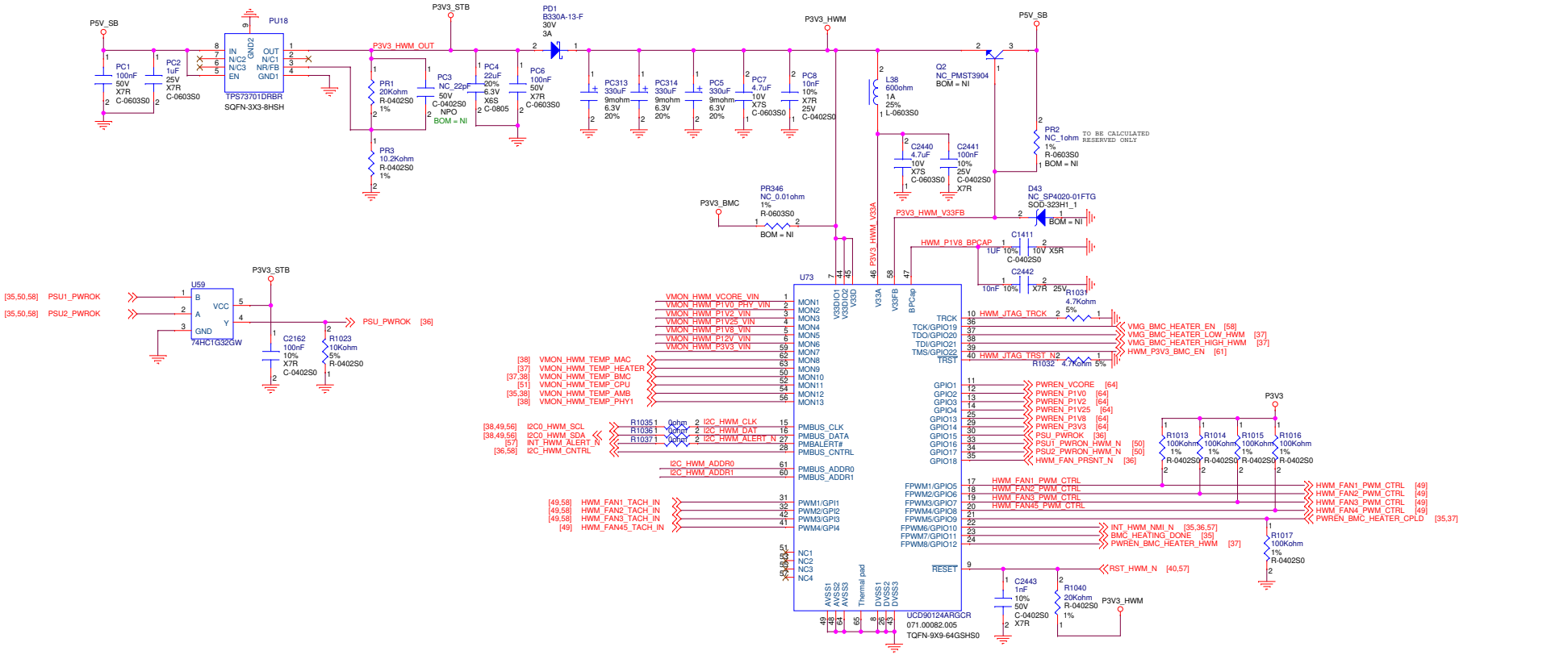


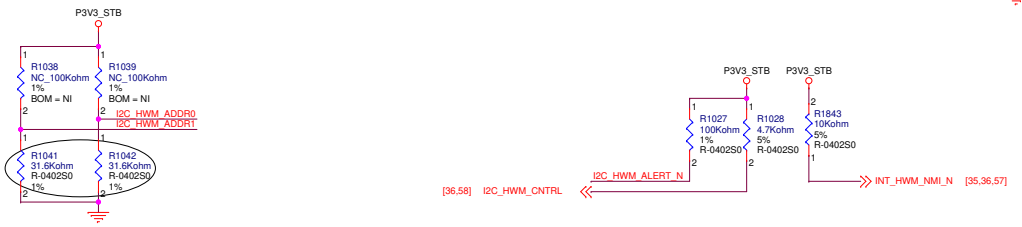
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UfiSpace Co., Ltd.

Title: 35. CPLD_10M04SAU169I7G

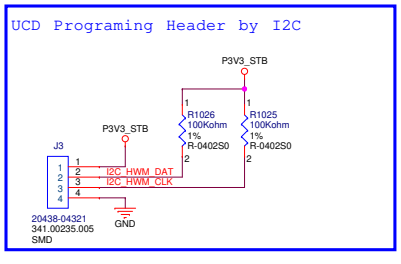
Document Number: T99O089T03 | Sheet 35 of 77 | Rev

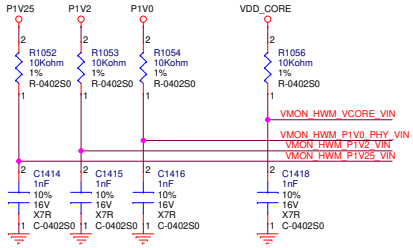
HWM MONITOR_UCD90124A

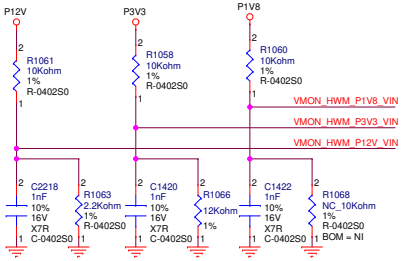




PMBus Add: 12x4+4=52 0x34







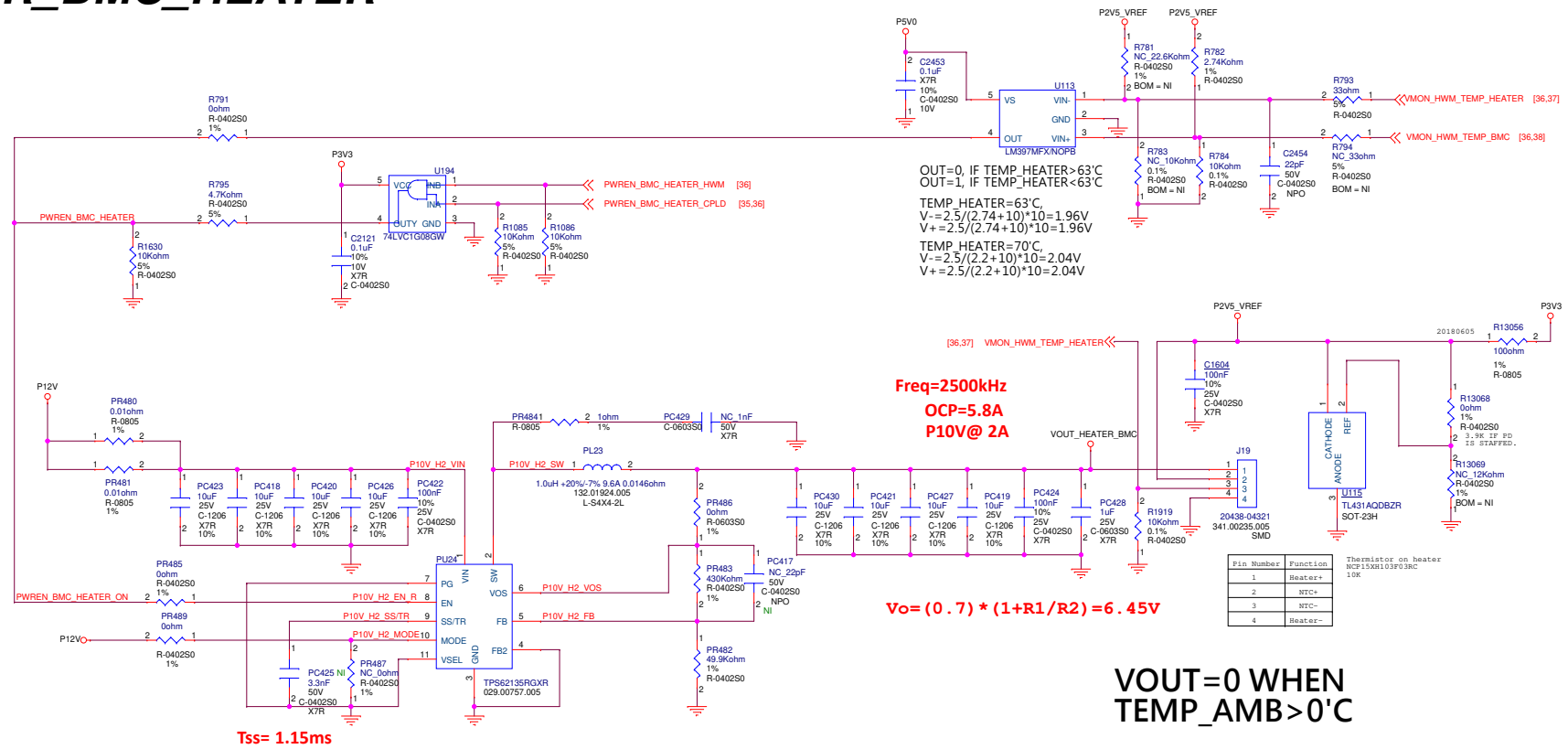
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UfiSpace Co., Ltd.

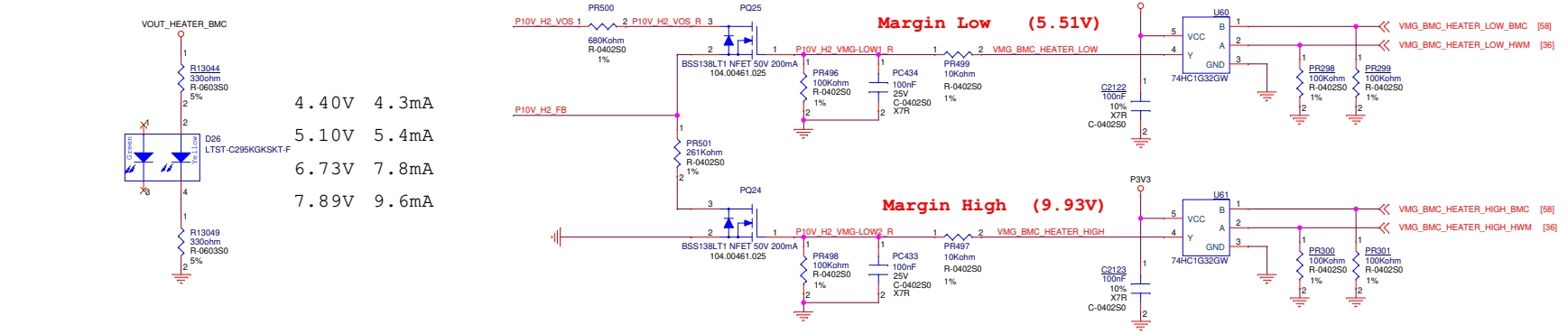
Title: 36. HWM_UCD90124A

Document Number: T99O089T03 | Sheet 36 of 77 | Rev

DC_PWR_BMC_HEATER



Pin Number	Function
1	Heater+
2	NTC+
3	NTC-
4	Heater-



	PWR (5~5.5 OHM HEATER)	VOUT	MARGIN HIGH	MARGIN LOW
8.6	8.2~9.0W	6.73V	L	L
11.9	11.3~12.5W	7.89V	H	L
3.7	3.5~3.9W	4.40V	L	H
5.0	4.7~5.2W	5.10V	H	H

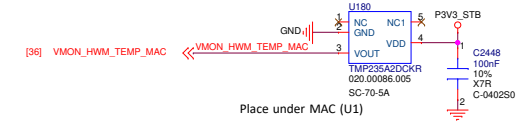
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UfiSpace Co., Ltd.

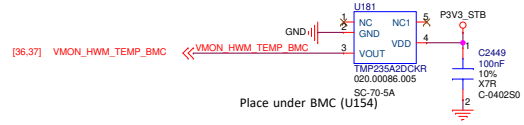
Title: 37. DC_PWR_BMC_HEATER

Document Number: T99O089T03 | Sheet 37 of 77 | Rev

THERMAL SENSOR

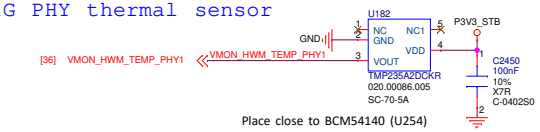


Place under MAC (U1)

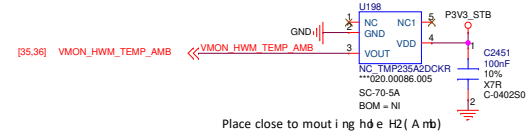


Place under BMC (U154)

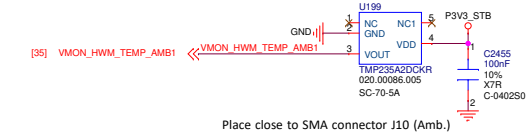
1G PHY thermal sensor



Place close to BCM54140 (U254)



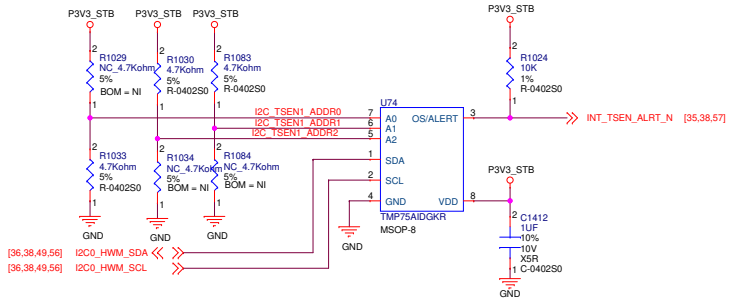
Place close to mout i ng hd e H2(A mb)



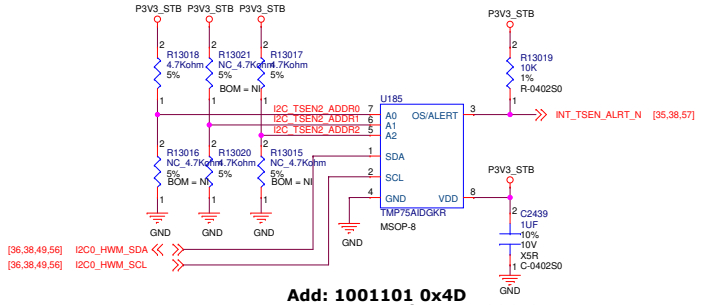
Place close to SMA connector J10 (Amb.)



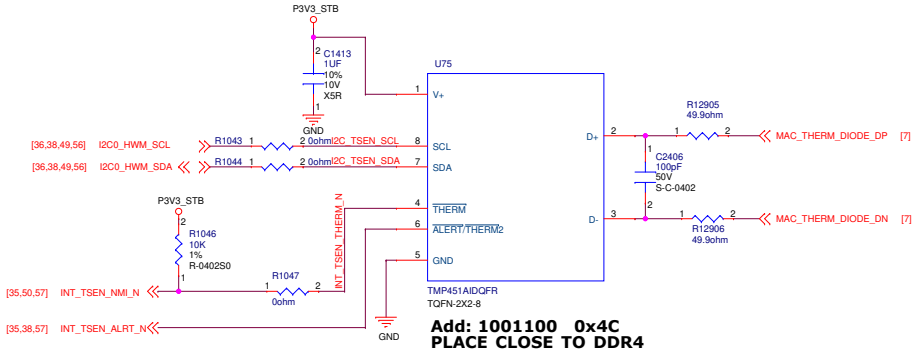
Place close to X14 (OCXO)



Add: 1001110 0x4E
PLACE UNDER BMC



Add: 1001101 0x4D
PLACE around CJ12 100G Cage



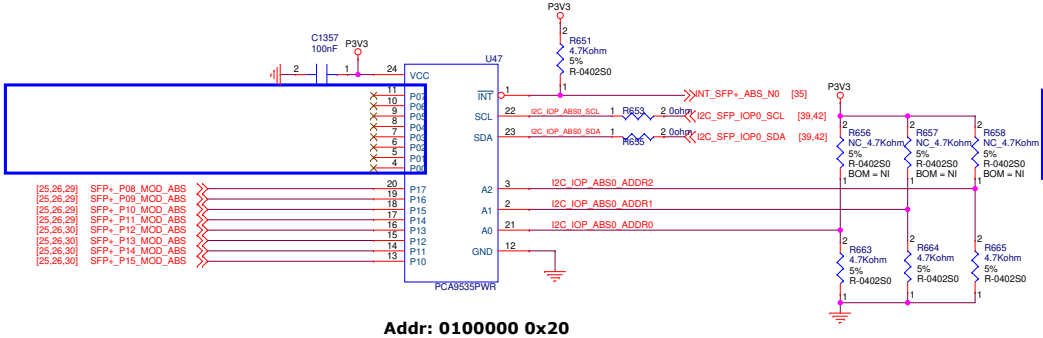
Add: 1001100 0x4C
PLACE CLOSE TO DDR4

ufiSpace UfiSpace Co., Ltd.

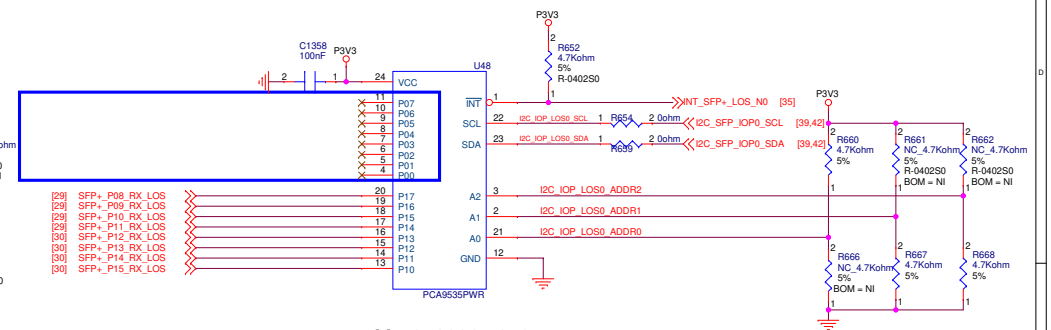
Title
38. THERMAL SENSOR

Document Number: PCB P/N: T99O089T03	Sheet 38 of 77	Rev

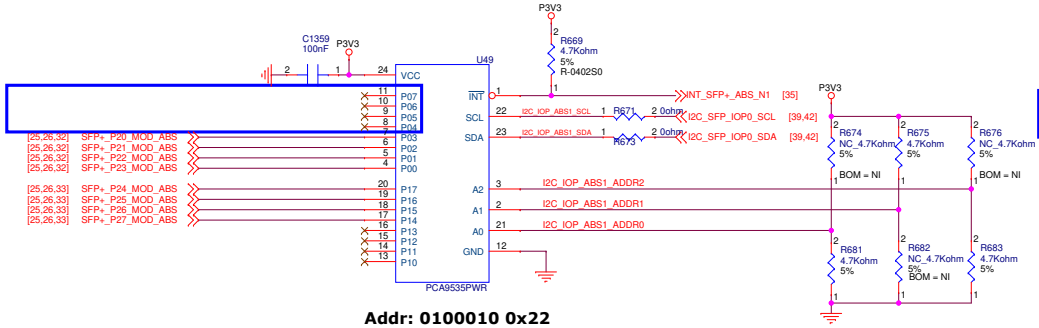
IO EXPANDER1



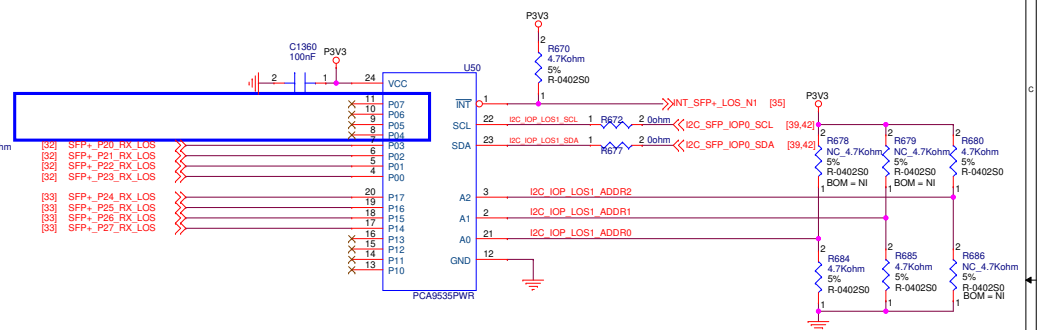
Addr: 0100000 0x20



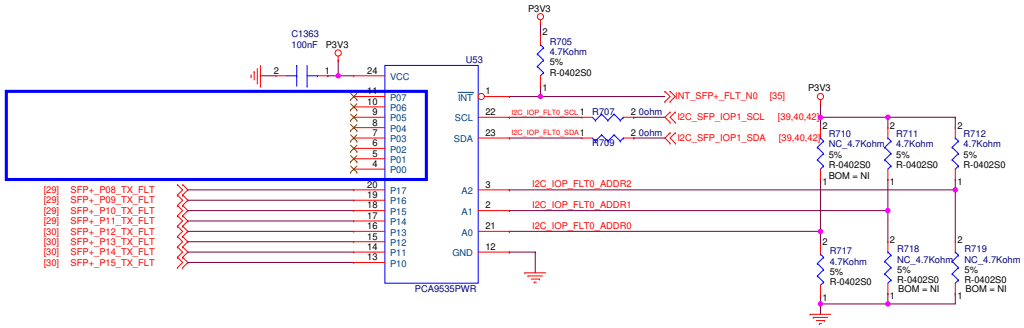
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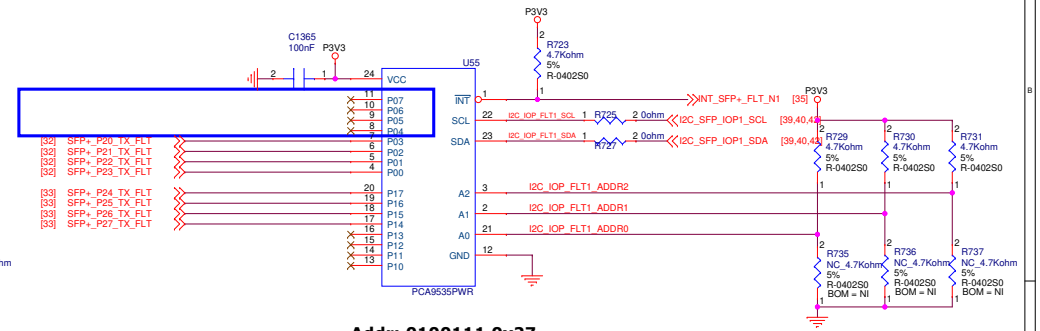
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Addr: 0100100 0x24



Addr: 0100110 0x26



Addr: 0100111 0x27

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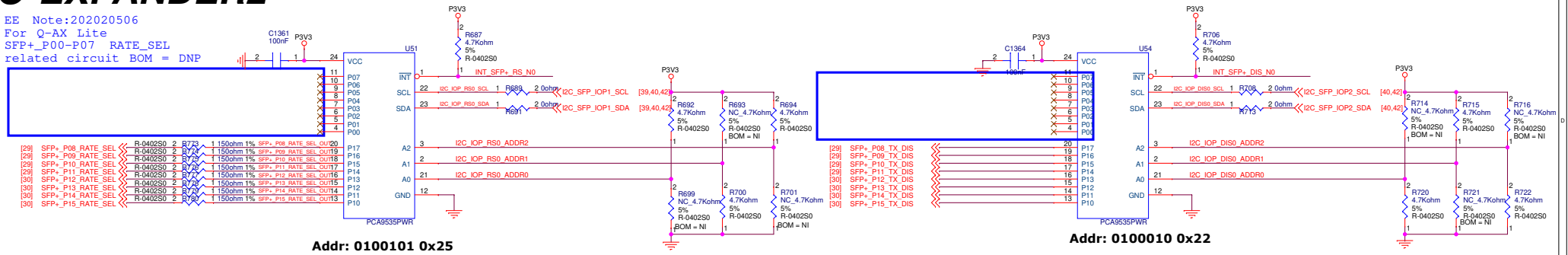
UfiSpace Co., Ltd.

Title: 39. IO EXPANDER1

Document Number: / PCB P/N:	Sheet	Rev
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IO EXPANDER2

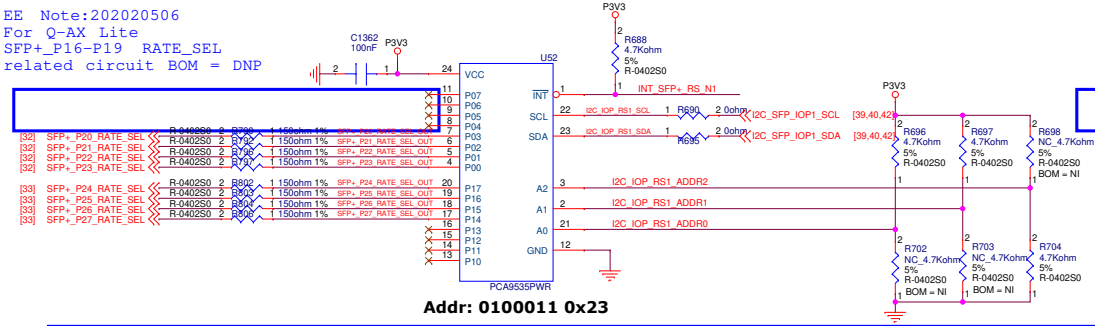
EE Note:202020506
For Q-AX Lite
SFP+_P00-P07 RATE_SEL
related circuit BOM = DNP



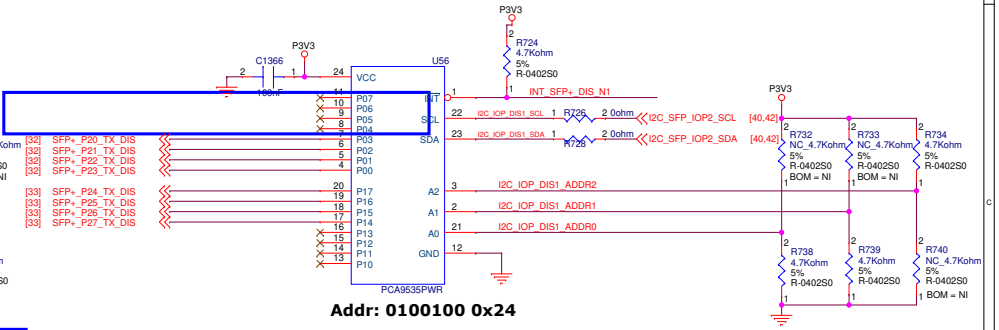
Addr: 0100101 0x25

Addr: 0100010 0x22

EE Note:202020506
For Q-AX Lite
SFP+_P16-P19 RATE_SEL
related circuit BOM = DNP

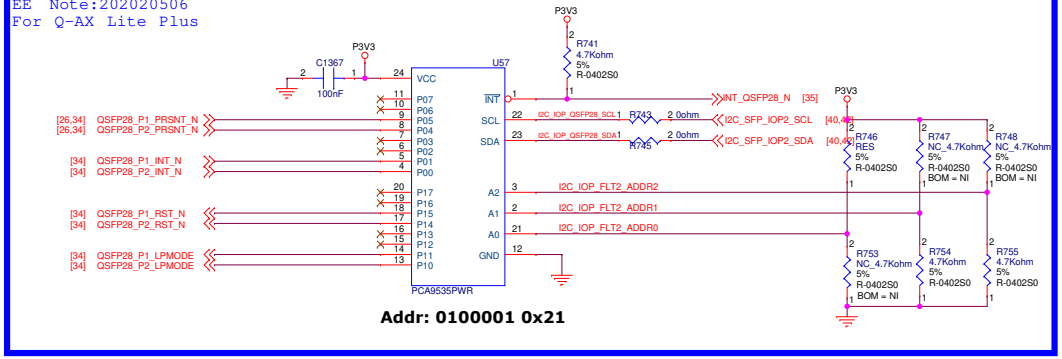


Addr: 0100011 0x23

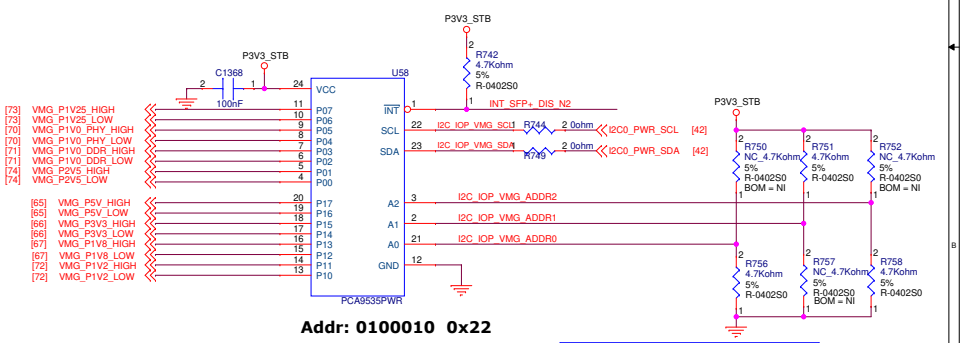


Addr: 0100100 0x24

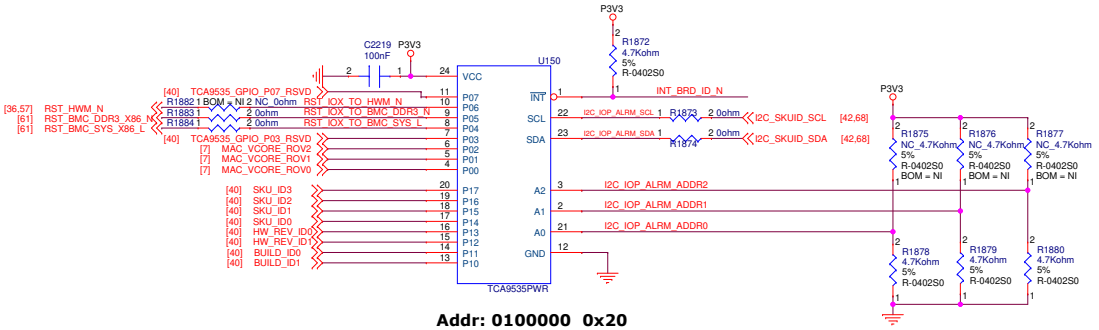
EE Note:202020506
For Q-AX Lite Plus



Addr: 0100001 0x21

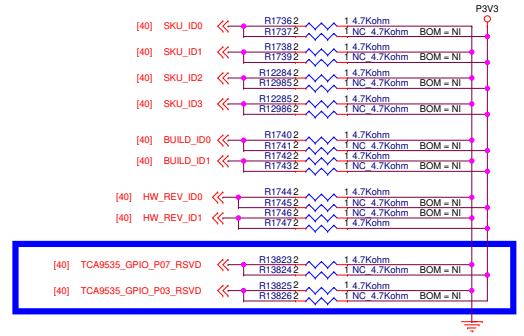


Addr: 0100010 0x22



Addr: 0100000 0x20

EE note:20200506
U150 change from PCA9535PWR to TCA9535PWR
for current leakage issue



EE note:20200506
Reserve U150.11 ,U150.7 for extension ID use

SKU ID [3:0]	
0000	CSGR_QAX_22XS
0001	CSGR_QAX_30XS
0010	CSGR_NTM_30XS
0011	RESERVED
0100	CSGR_QUX_28SMT
0101	CSGR_QUX_18SMT
0110	CSGR_QUX_16SMT
0111	CSGR_QUX_12SMT
1000 ~ 1011	RESERVED
1100 ~ 1111	CSGR SERIES

Build Rev [1:0]	
00	0
01	1
10	2
11	3

Hardware Revision [1:0]	
00	Proto
01	Alpha
10	Beta
11	PVT

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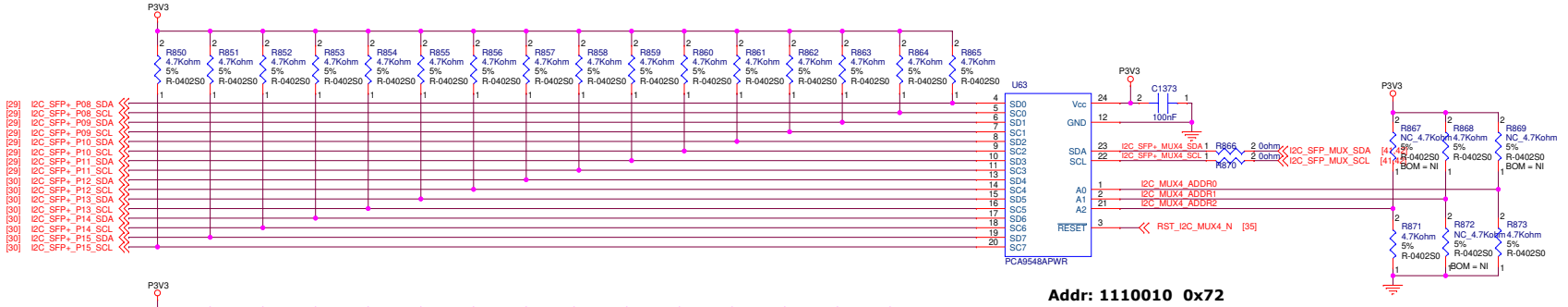
UfiSpace Co., Ltd.

Title: 40. IO EXPANDER2

Document Number: T99O089T03
PCB P/N:
Sheet 40 of 77
Rev

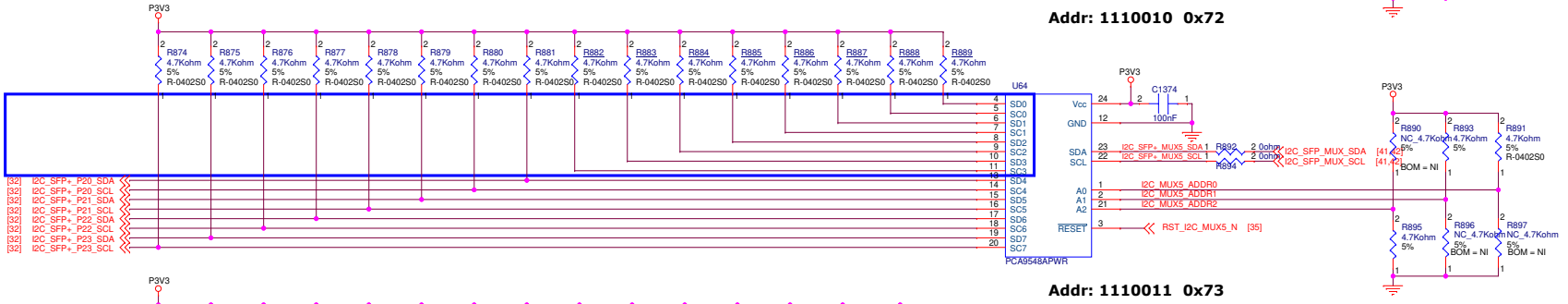
I2C MUX1

EE Note:20200602
For QAX_Lite sku
Remove
SFP+_P00-P07 I2C MUX and related circuit

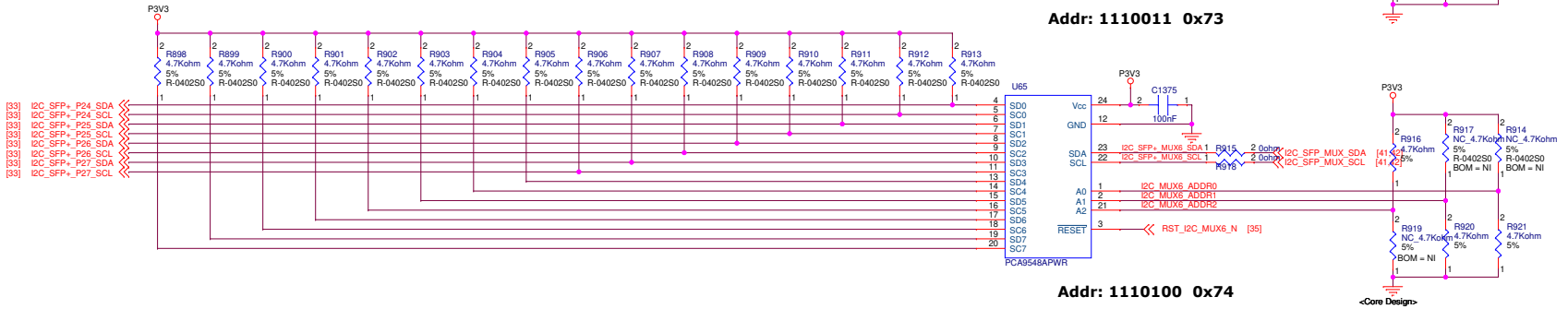


Addr: 1110010 0x72

EE Note:20200602
For QAX_Lite sku
Remove
SFP+_P16-P19 I2C



Addr: 1110011 0x73



Addr: 1110100 0x74

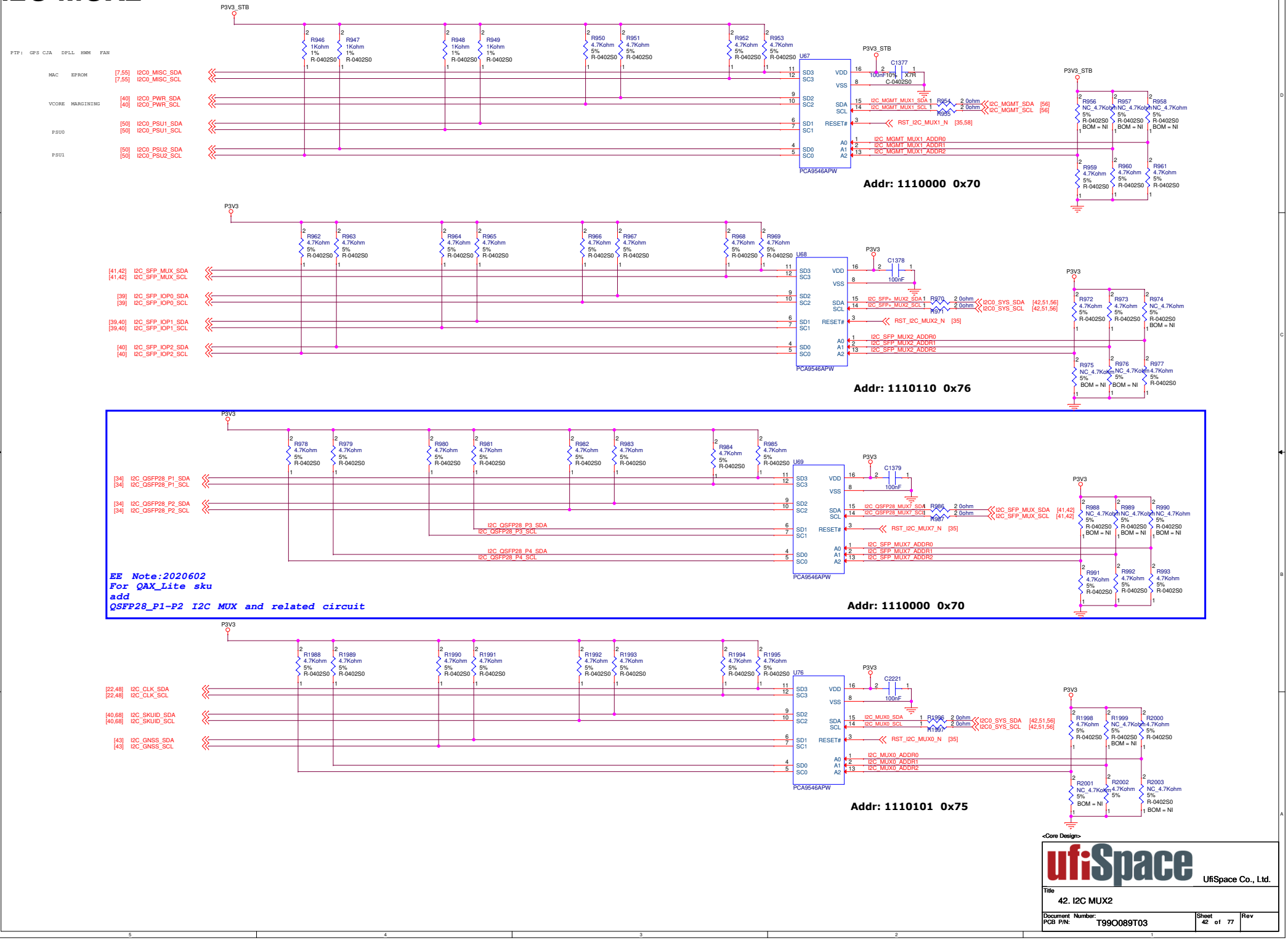
<Core Design>

UfiSpace Co., Ltd.

Title: 41. I2C MUX1

Document Number: T99O089T03 | Sheet 41 of 77 | Rev
PCB P/N:

I2C MUX2



<Core Design>

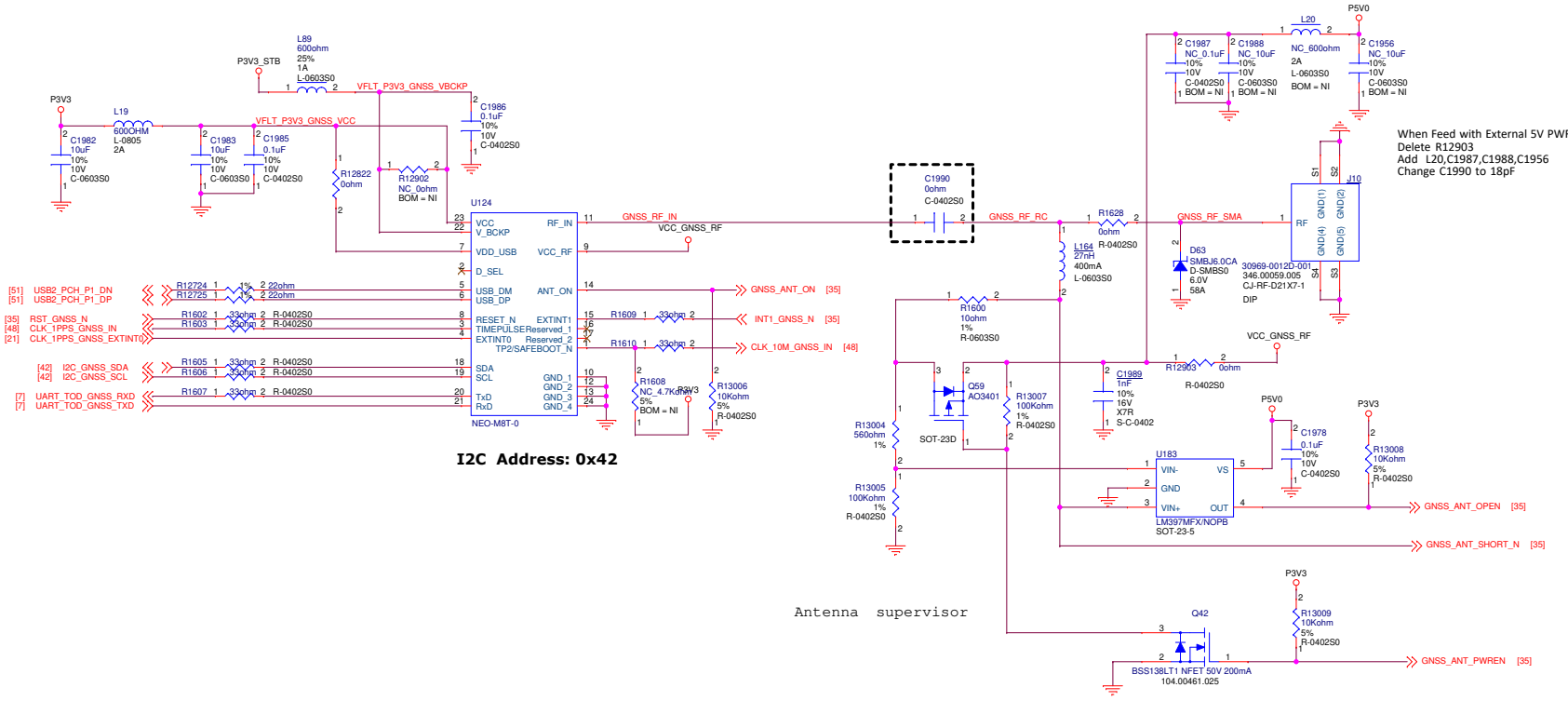
UfiSpace Co., Ltd.

Title

42. I2C MUX2

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PTP_GNSS MODULE



I2C Address: 0x42

1. CPU configure GNSS module to set ANT_ON=1 during initialization.
2. CPLD set ANT_PWREN=1 when receive ANT_ON=1 signal from GNSS.
3. CPLD issue PTP interrupt if ANT_SHORT_N=0.
4. CPLD turn on/off GNSS LED per ANT_SHORT_N status.
5. ANT_OPTEN=1, NO ANTENNA IS INSTALLED OR PASSIVE ANTENNA IS PLUGED.
6. ANT_OPTEN=0, ACTIVE ANTENNA IS INSTALLED.

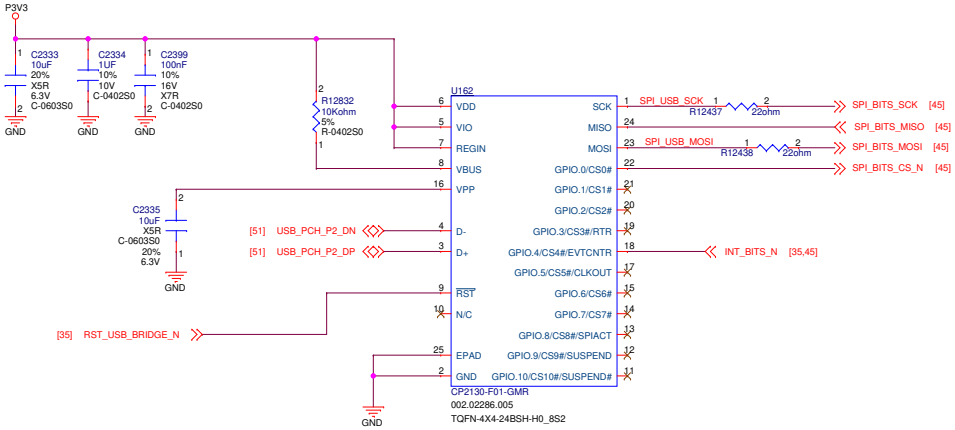
<Core Design>

UfiSpace Co., Ltd.

Title: 43. PTP_GNSS MODULE

Document Number:	Sheet	Rev
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PTP_USB TO SPI BRIDGE



<Core Design>

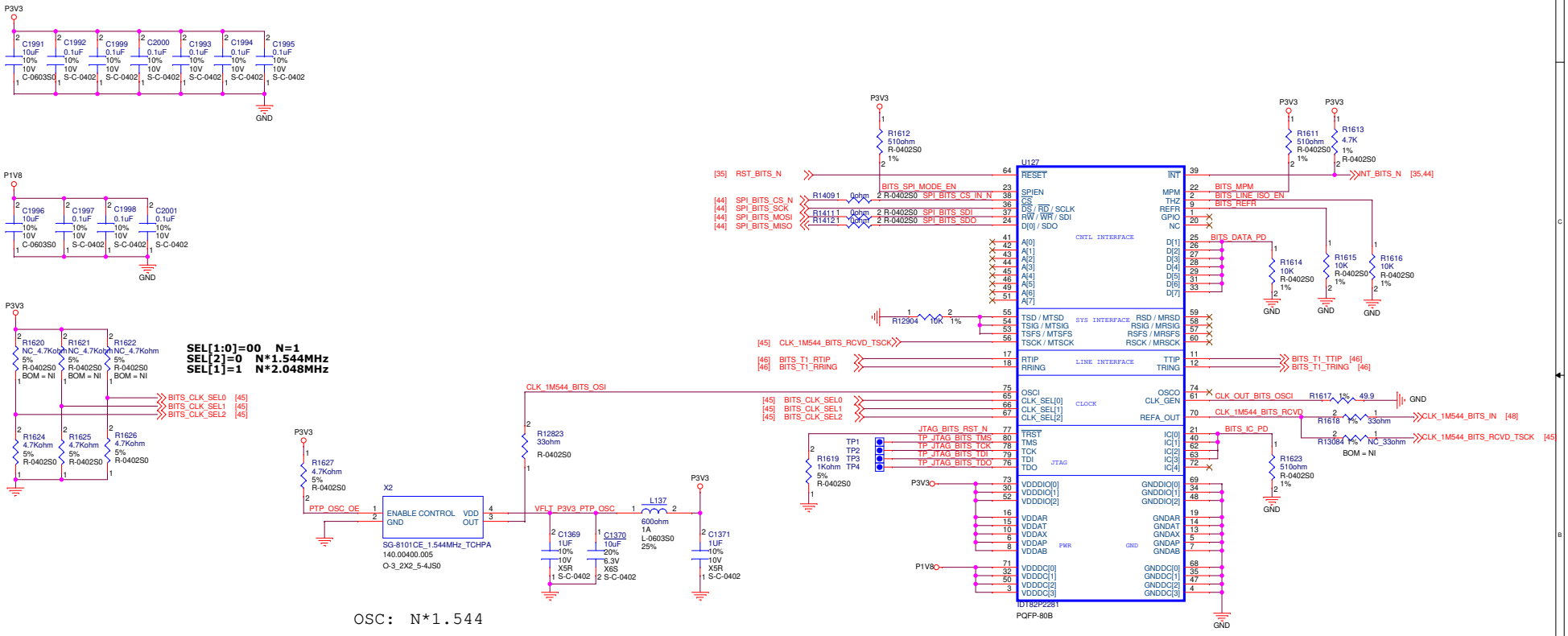
UfiSpace Co., Ltd.

Title

44. PTP_USB TO SPI BRIDGE

Document Number:	Sheet	Rev
PCB P/N: T99O089T03	44 of 77	

PTP_T1/E1 RECEIVER



<Core Design>

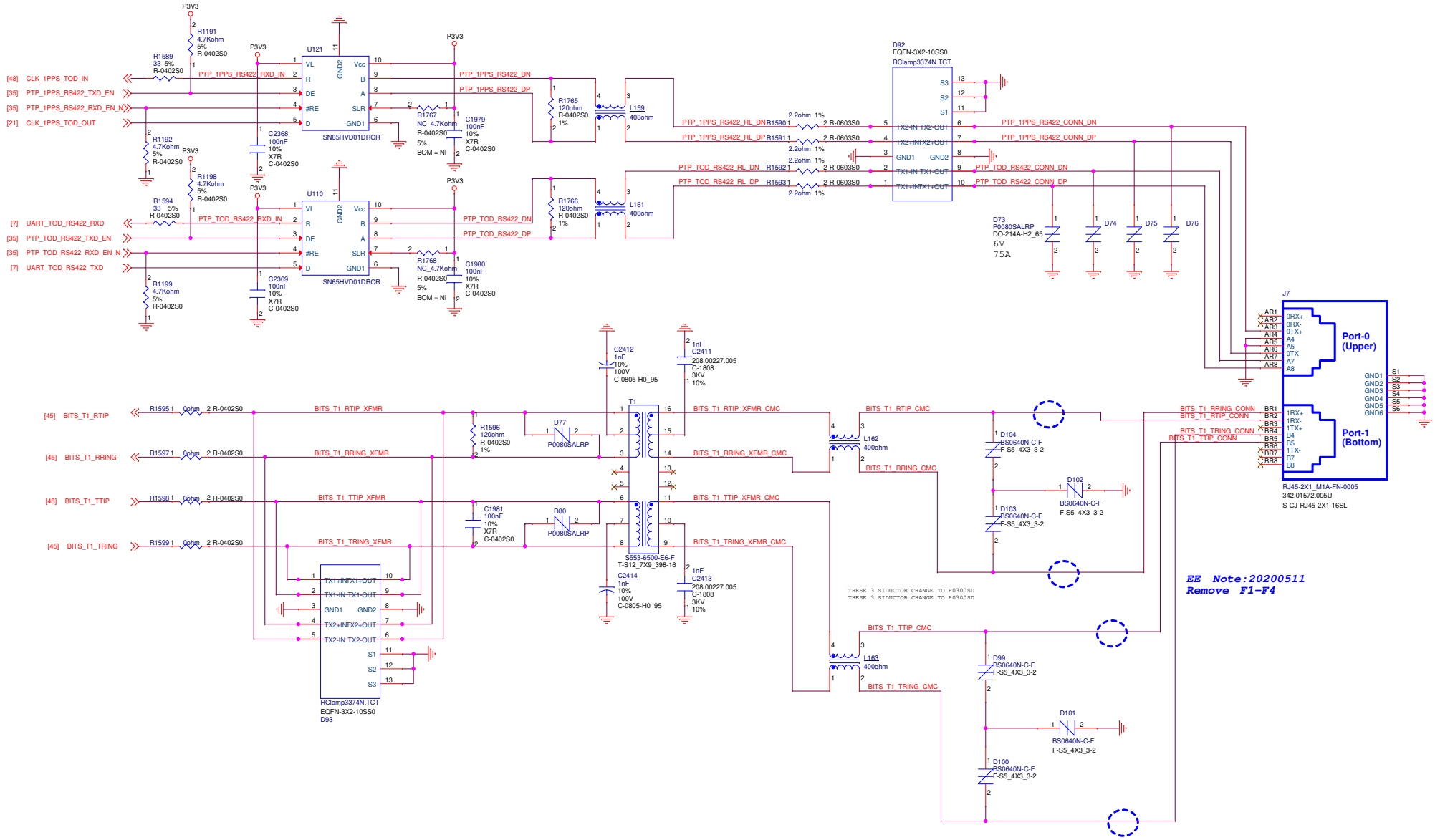
UfiSpace Co., Ltd.

Title

45. PTP_T1/E1 RECEIVER

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T1/E1 & TOD IN/OUT



<Core Design>

UfiSpace Co., Ltd.

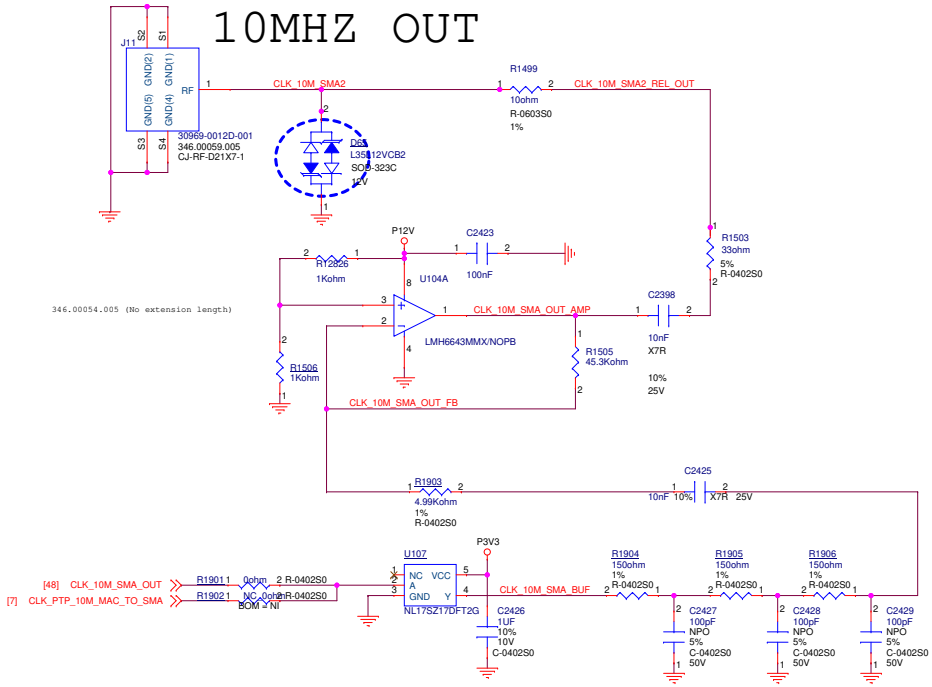
Title

46. PTP_T1/E1 & TOD IN/OUT

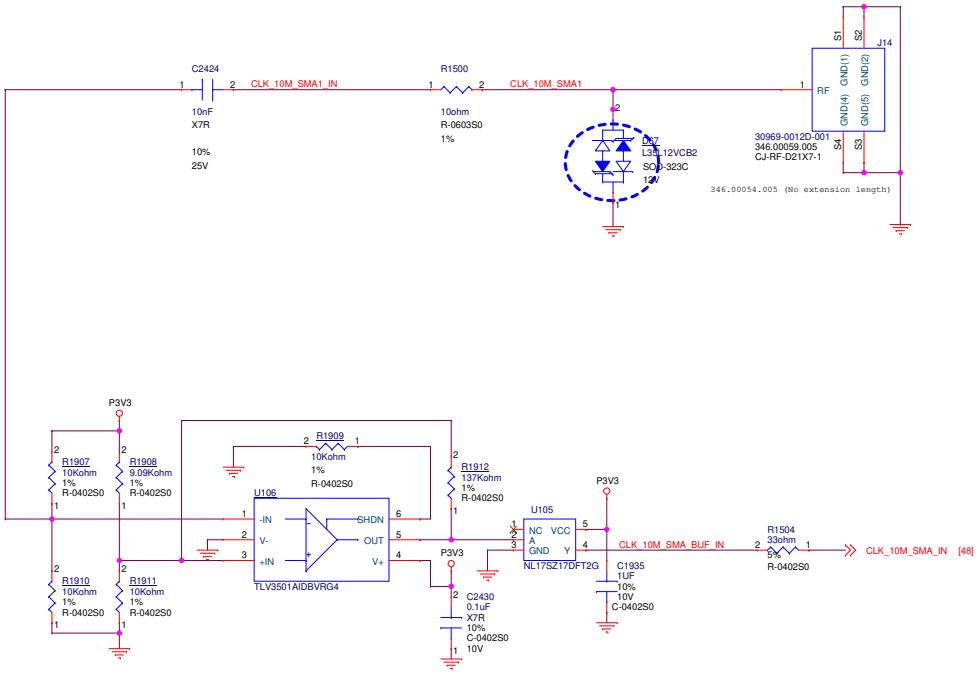
Document Number:	Sheet	Rev
PCB P/N: T99O089T03	46 of 77	

PTP_1PPS & 10MHZ IN/OUT

10MHZ OUT

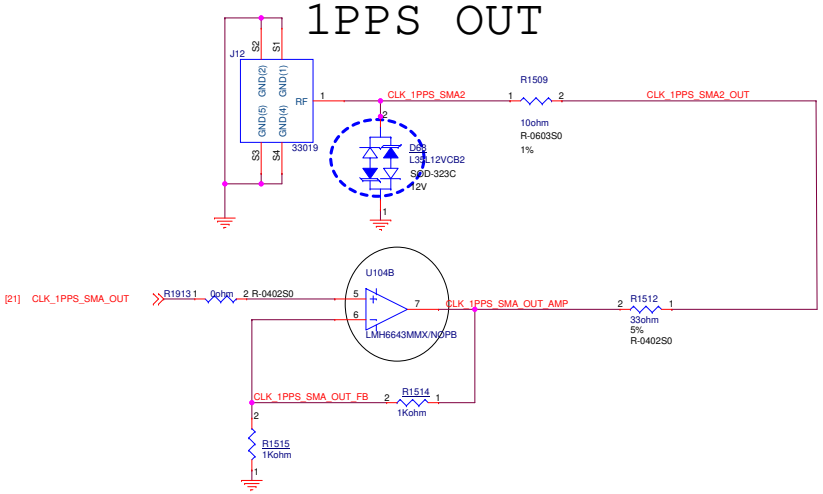


10MHZ IN

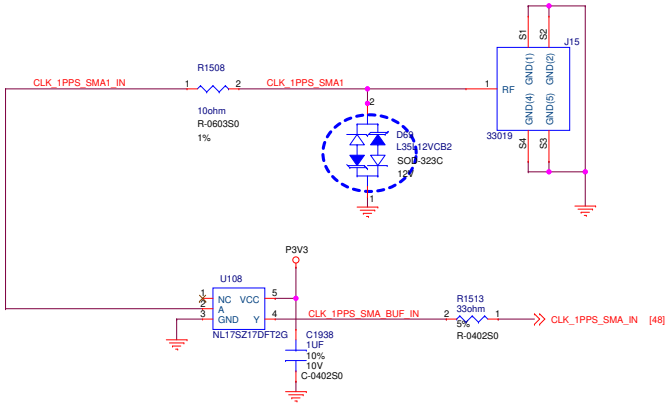


EE note: 20200504
Change D65,D67~D69 from AZ1355-04S.R7G to L35L12VCB2 P3V3 leakage issue

1PPS OUT



1PPS IN



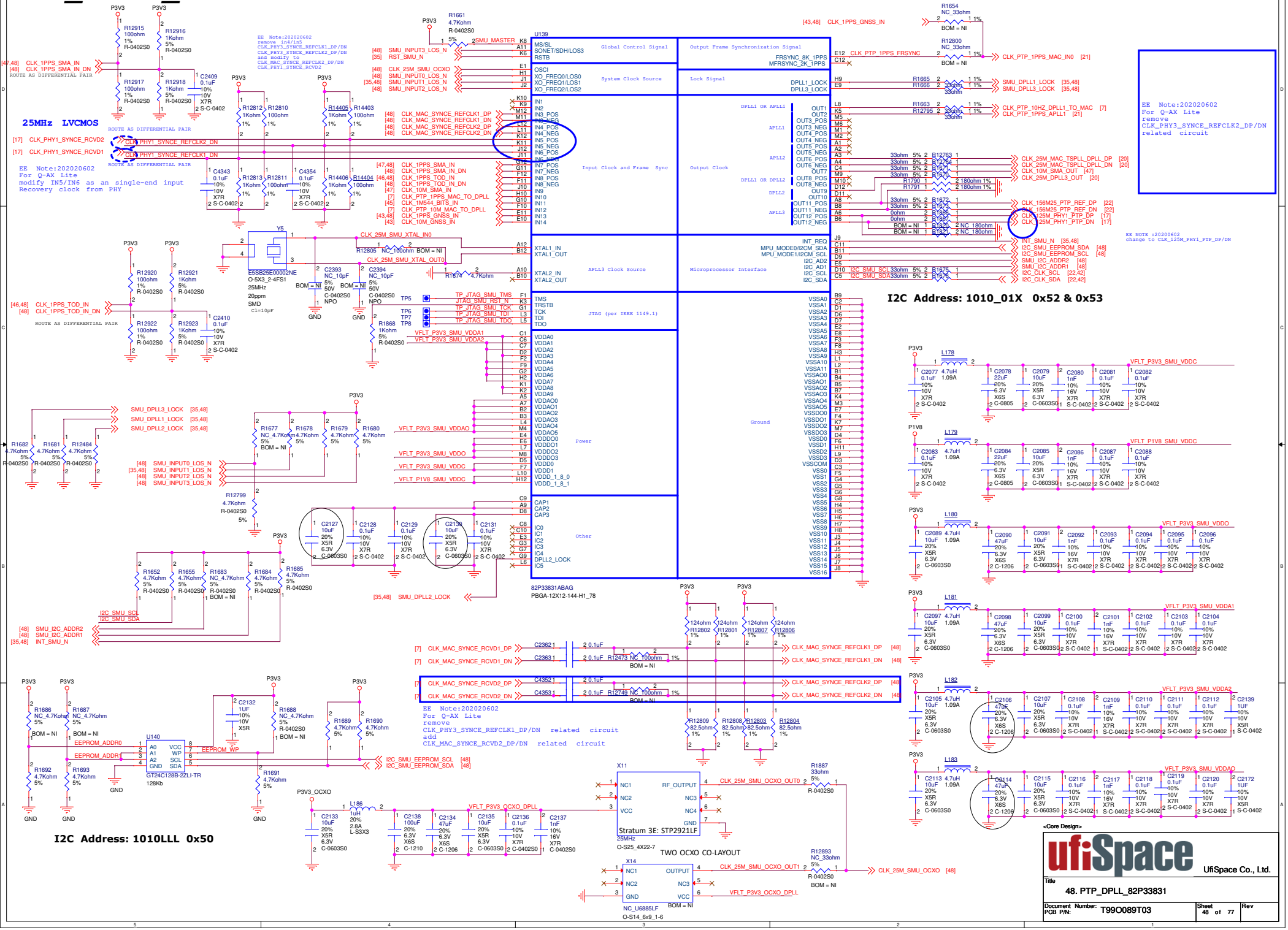
<Core Design>

UfiSpace Co., Ltd.

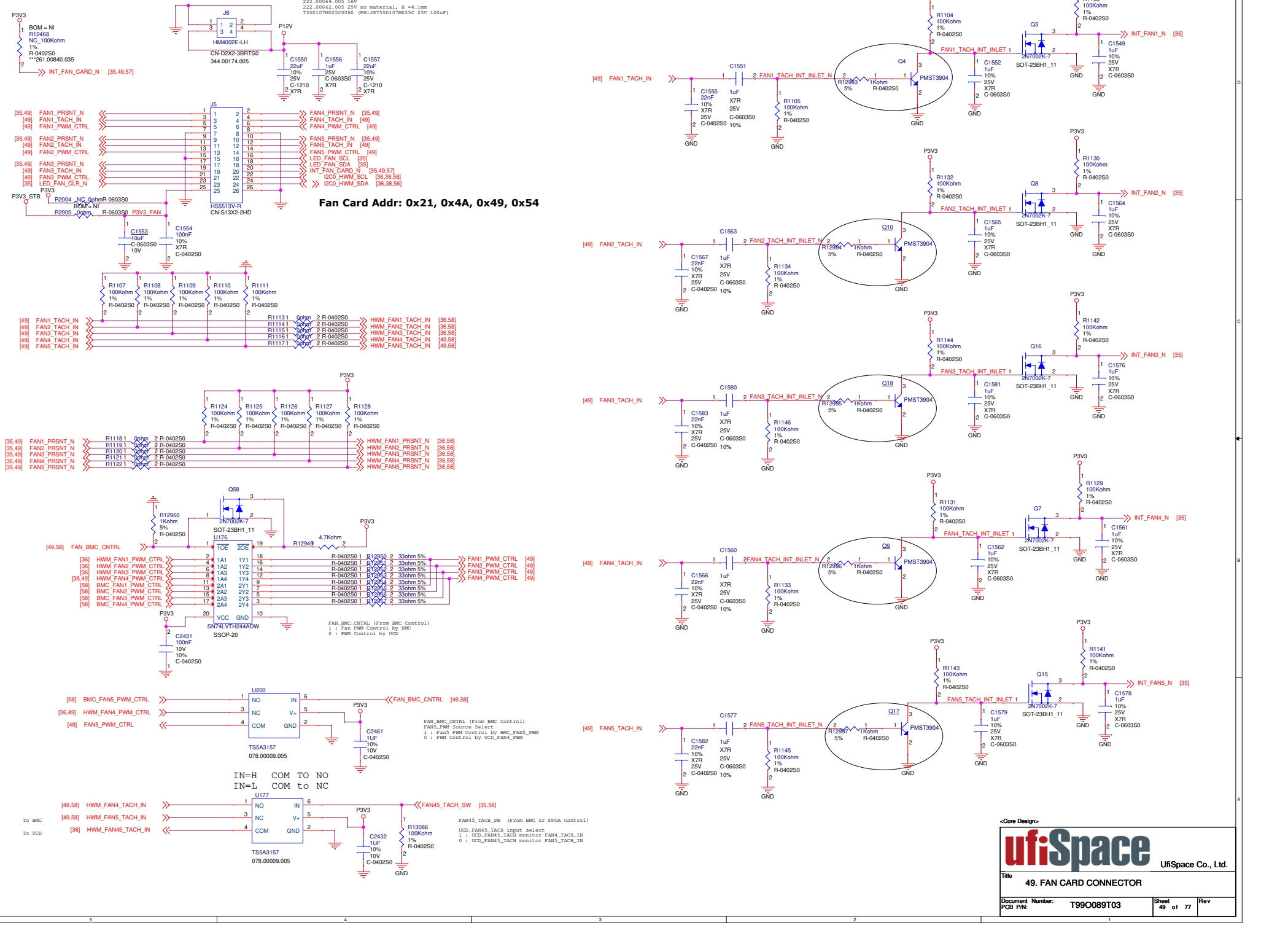
Title
47. PTP_1PPS & 10MHZ IN/OUT

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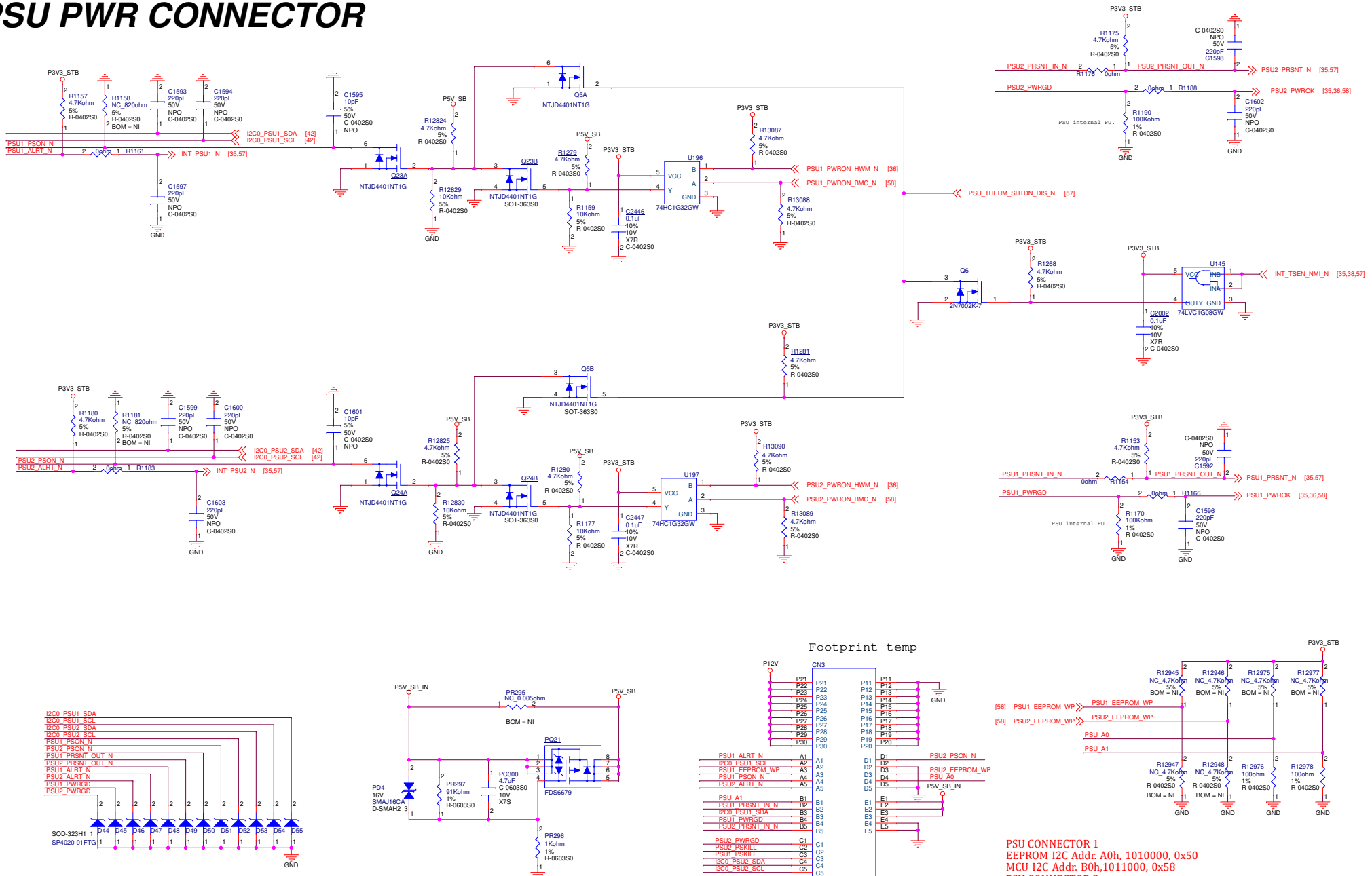
PTP_DPLL_82P33831



FAN CARD CONNECTOR



PSU PWR CONNECTOR



PSU CONNECTOR 1
EEPROM I2C Addr. A0h, 1010000, 0x50
MCU I2C Addr. B0h,1011000, 0x58
PSU CONNECTOR 2
EEPROM I2C Addr. A0h, 1010000, 0x50
MCU I2C Addr. B0h,1011000, 0x58

<Core Design>

UfiSpace Co., Ltd.

Title: 50. PSU PWR CONNECTOR

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CPU PCIE X16 CONNECTOR

CPU Card I2C Addr: 0x44, 0x8, 0x51, 0x4F, 0x77, 0x48

A1 TIE TO B81 ON CPU CARD

B81 TIE TO A1 ON CPU CARD

J1 PCIe_Gen3_CONN

98317C-164-2MMF
CN-EXPPCI-164A

2018/03/29:
USB2_PCH_P0: USB MUX
USB2_PCH_P1: BMC
USB2_PCH_P2: USB to SPI
USB2_PCH_P3: GPS

<Core Design>

UfiSpace Co., Ltd.

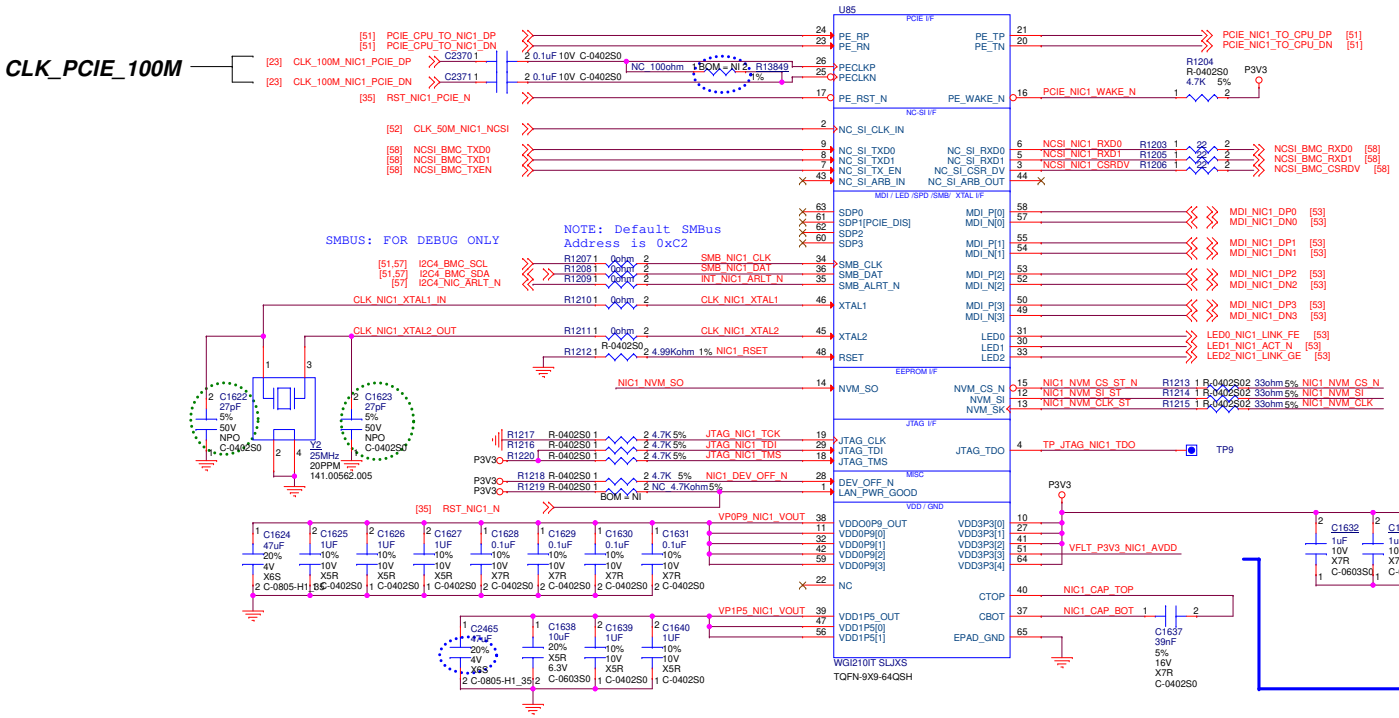
Title: 51. CPU_PCIE X16 CONNECTOR

Document Number: T99O089T03 | Sheet 51 of 77 | Rev

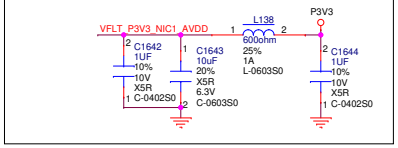
CPU_NIC1_I210-IT

EE Note: 20200513
ADD R13849 reserve for Clock voltage fine tune

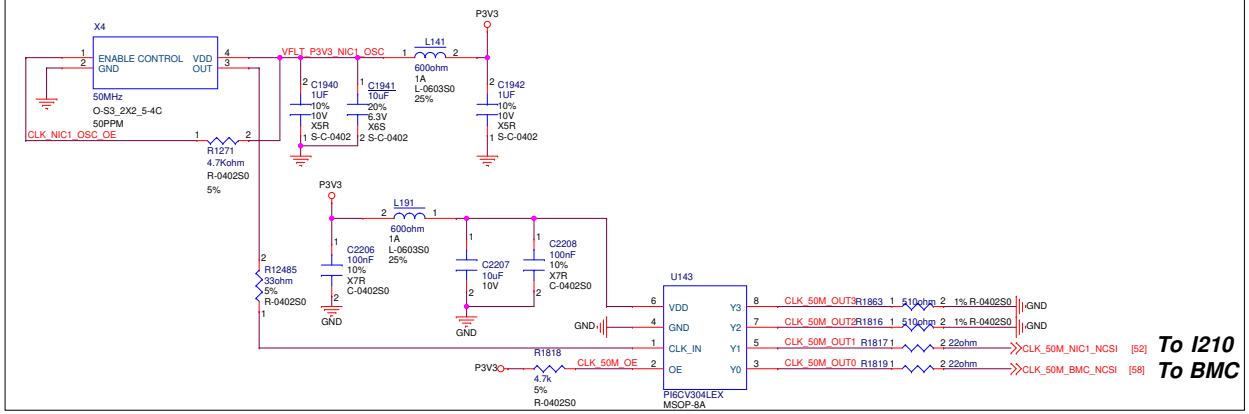
CLK_PCIE_100M



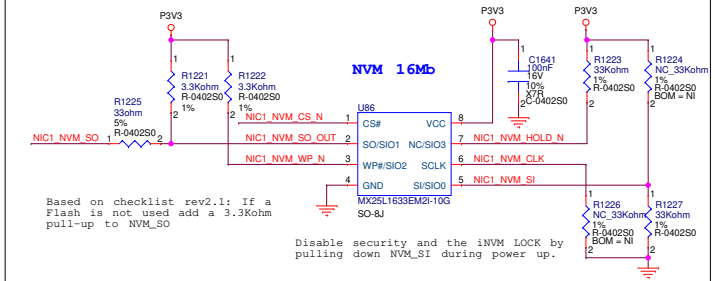
VFLT_P3V3_NIC1_AVDD



NCSI_50M_CLK Clock Buffer



I210 SPI Flash



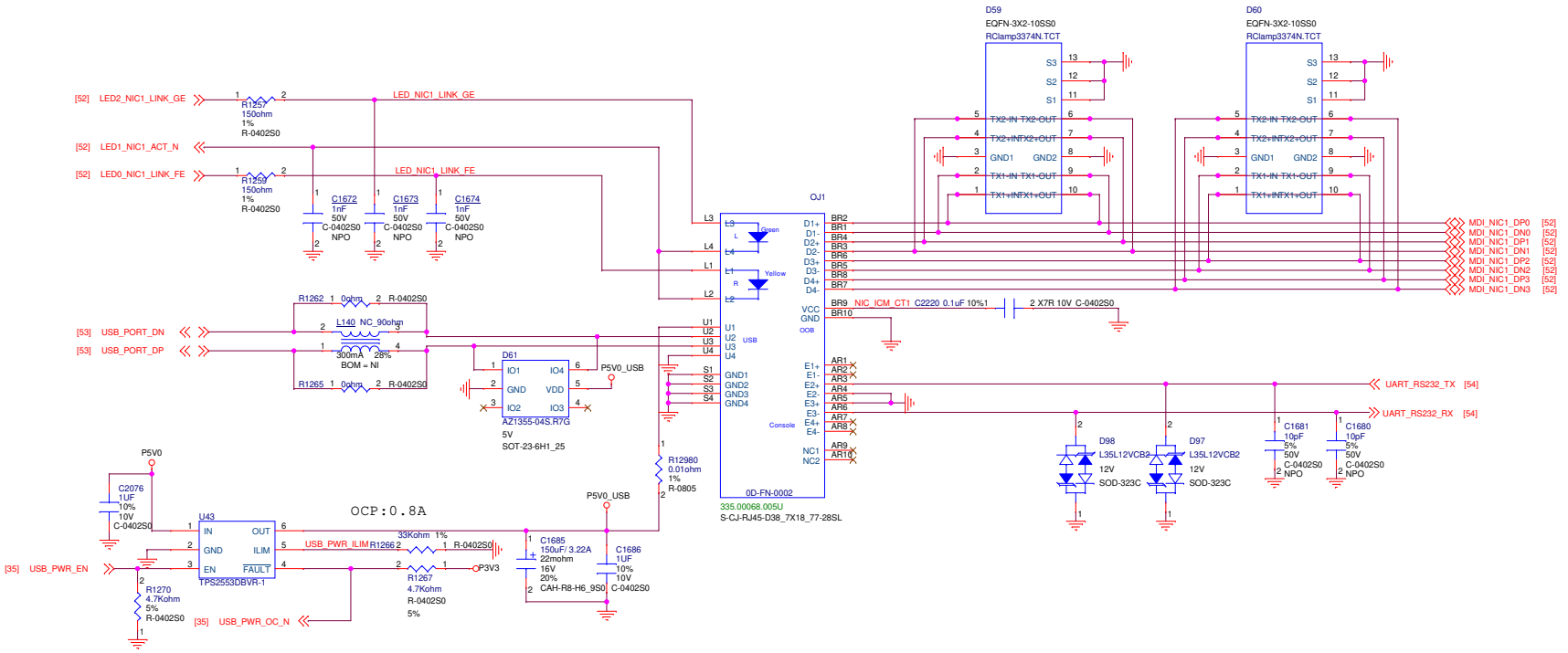
<Core Design>

UfiSpace Co., Ltd.

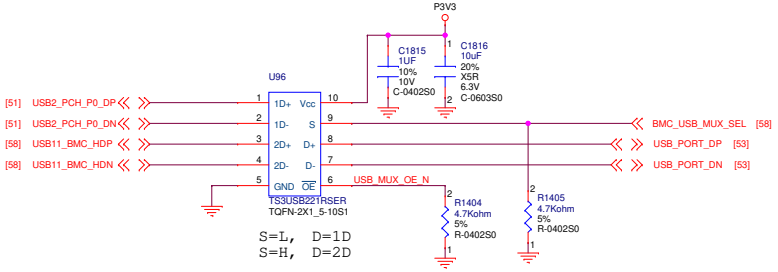
Title: 52. CPU_NIC1_I210-IT			
Document Number: T99O089T03	PCB P/N:	Sheet 52 of 77	Rev

GBE OOB & USB PORT

Front Port_GBE OOB and USB



USB Host select



Bus Switch for Front USB port Host select

	BMC_USB_MUX_SEL (Control from BMC)	USB Host
default	0	CPU
	1	BMC

<Core Design>

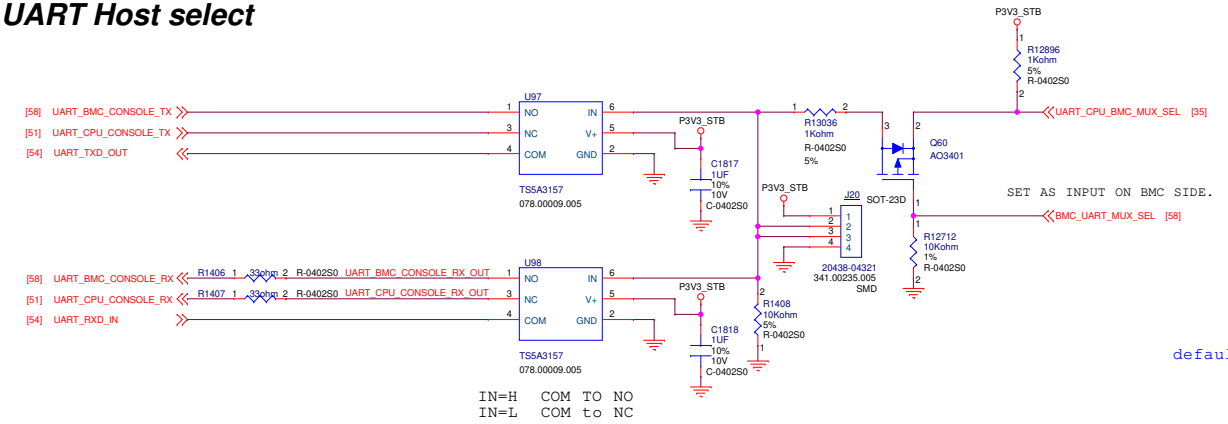
UfiSpace Co., Ltd.

Title: 53. GBE OOB & USB PORT

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CONSOLE MUX & RS232 XCVR

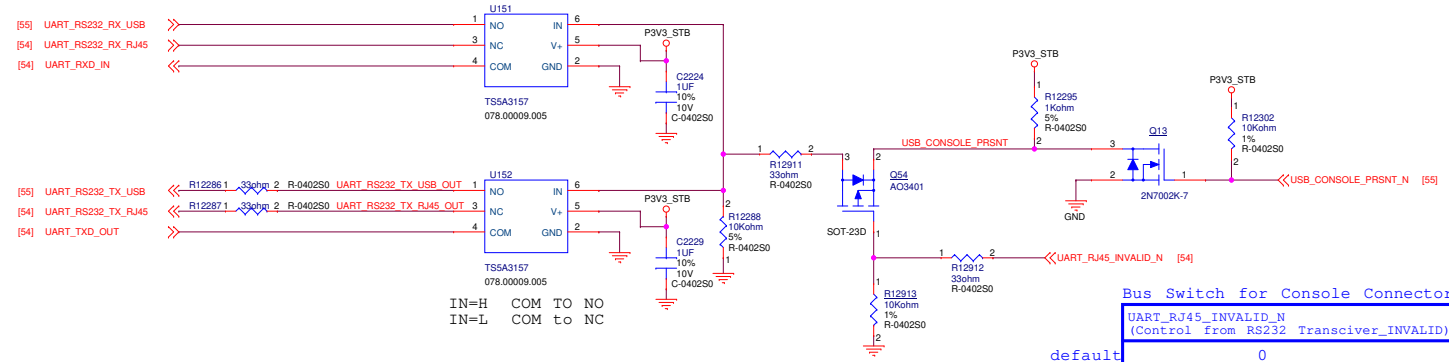
UART Host select



Bus Switch for UART Host select

BMC_UART_MUX_SEL (Control from BMC)	UART_CPU_BMC_MUX_SEL (Control from CPLD	UART Host
default 0	X	CPU
1	0	BMC
1	1	CPU

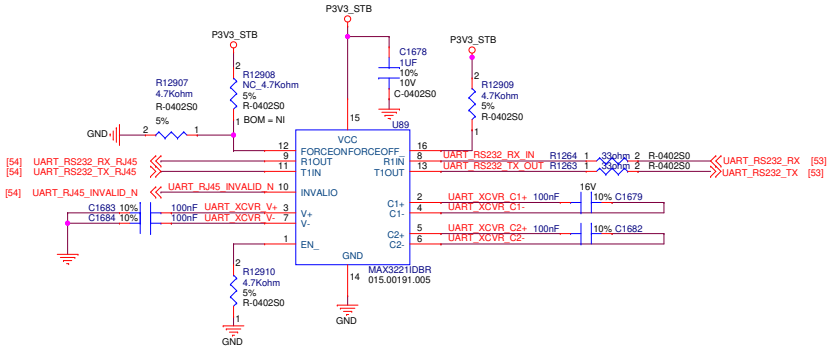
Console Output Connector Type Select



Bus Switch for Console Connector Type select

UART_RJ45_INVALID_N (Control from RS232 Transciver_INVALID)	USB_CONSOLE_PRSNT_N (Control by LED board insert)	Front Port Console Output
default 0	X	RJ45
1	0	USB
1	1	RJ45

RS232 Transciver for RJ45 Console Port



<Core Design>

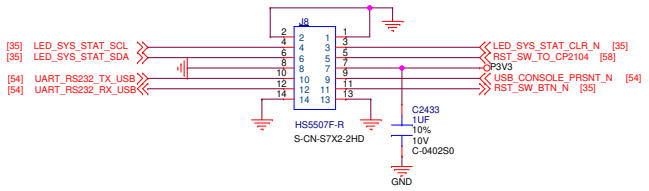
UfiSpace Co., Ltd.

Title: 54. CONSOLE MUX & RS232 XCVR

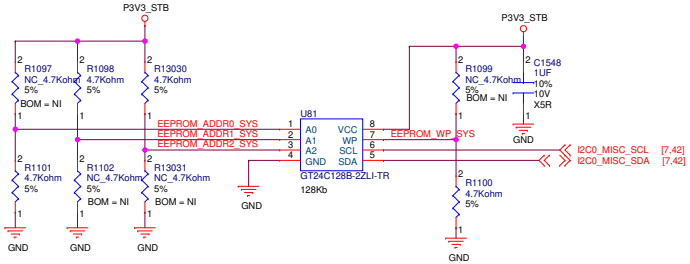
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LED CARD HEADER & EEPROM

LED CARD HEADER



EEPROM



Addr: 1010110 0x56

<Core Design>

UfiSpace Co., Ltd.

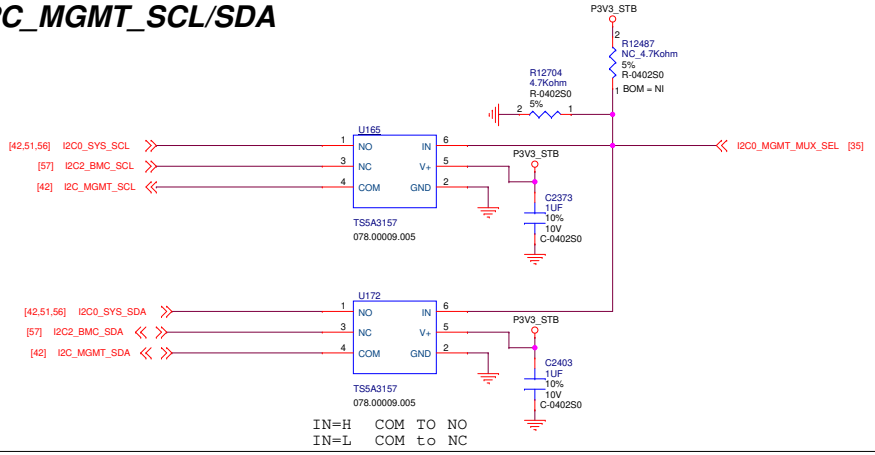
Title

55. LED CARD HEADER & EEPROM

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BMC & CPU I2C MUX

I2C_MGMT_SCL/SDA

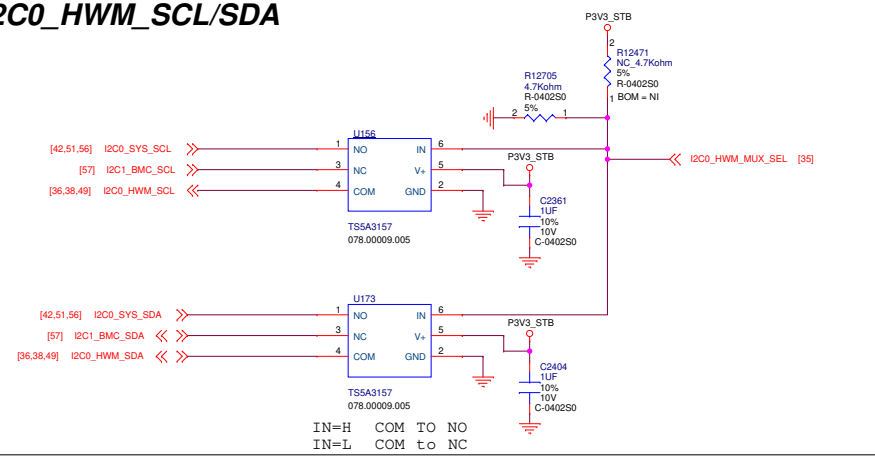


MGMT I2C Host select

default

I2C_MGMT_MUX (Control by CPLD)	MGMT I2C Host
0	BMC I2C
1	CPU I2C

I2C0_HWM_SCL/SDA

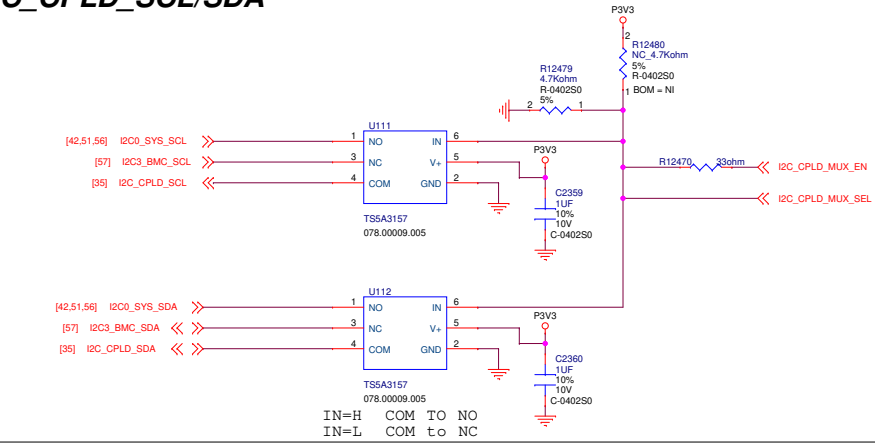


HWM I2C Host select

default

I2C_HWM_MUX (Control by CPLD)	HWM I2C Host
0	BMC I2C
1	CPU I2C

I2C_CPLD_SCL/SDA



CPLD I2C Host select

default

I2C_CPLD_MUX_EN (Control by CPLD)	I2C_CPLD_MUX_SEL (Control by BMC)	CPLD I2C Host
0	0	BMC I2C
0	1	BMC I2C
1	0	BMC I2C
1	1	CPU I2C

<Core Design>

UfiSpace Co., Ltd.

Title: 56. BMC & CPU I2C MUX

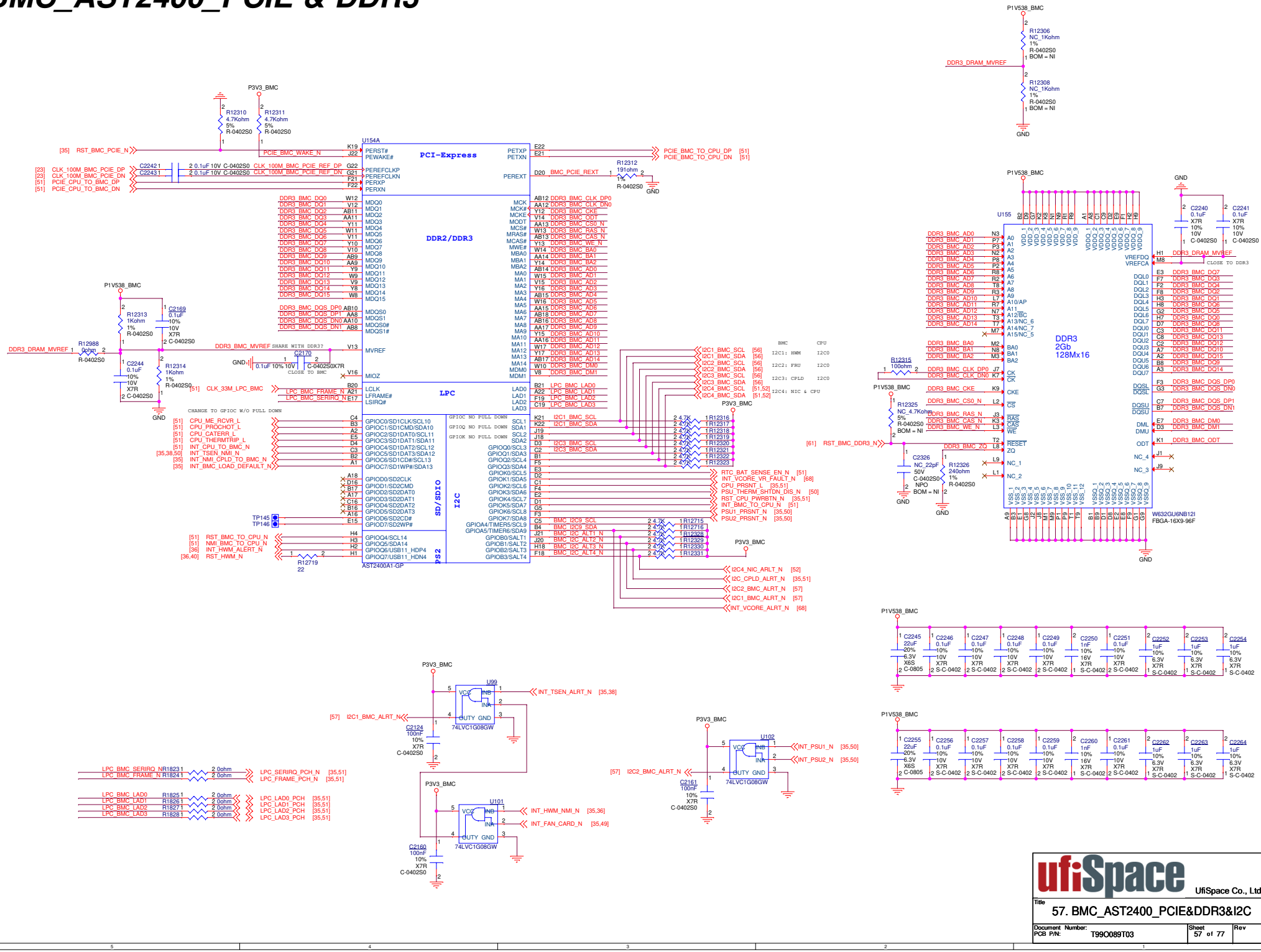
Document Number: T99O089T03

PCB P/N:

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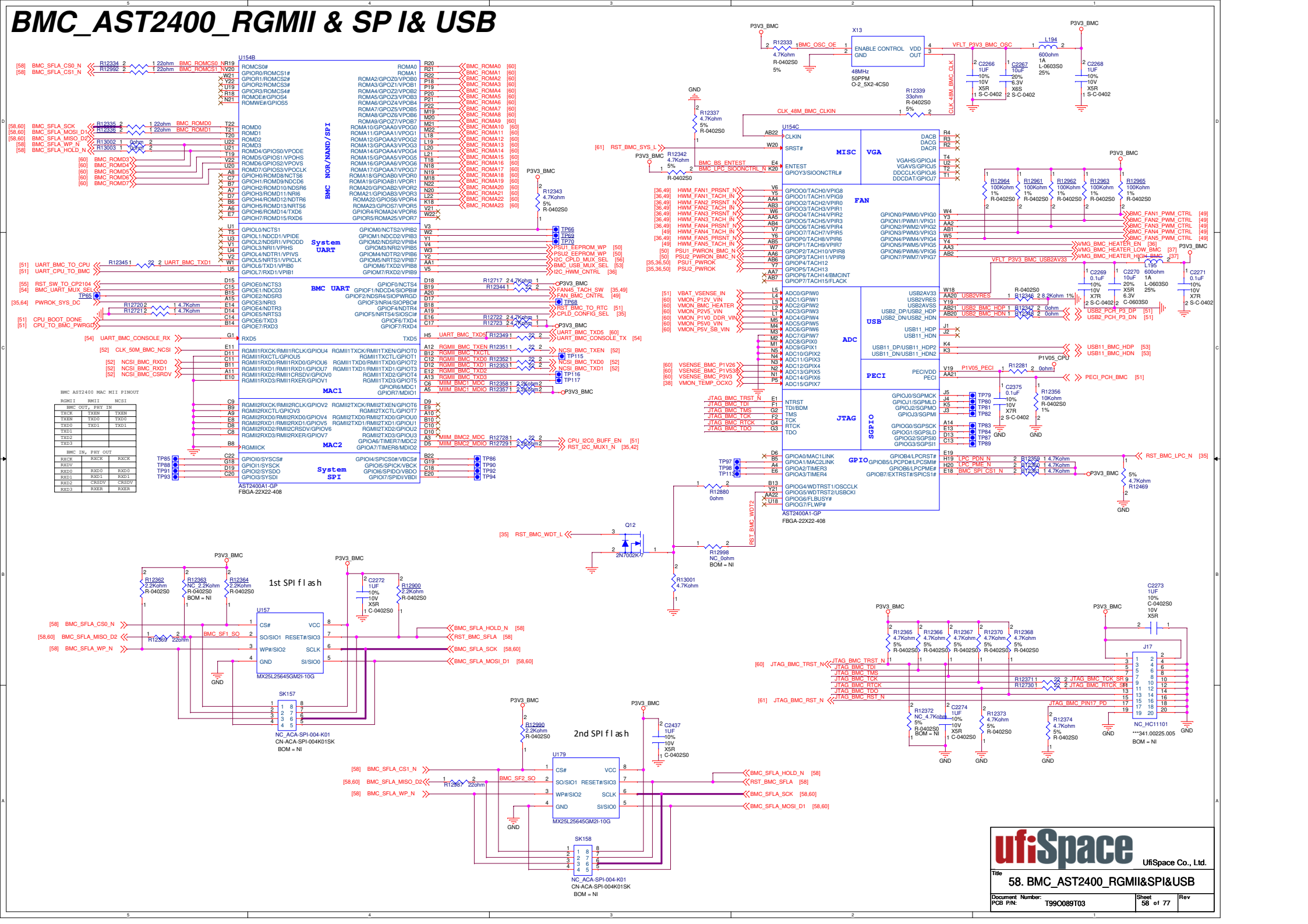
Rev

BMC_AST2400_PCIE & DDR3



UfiSpace Co., Ltd.	
Title	57. BMC_AST2400_PCIE&DDR3&I2C
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BMC_AST2400_RGMII & SP I& USB



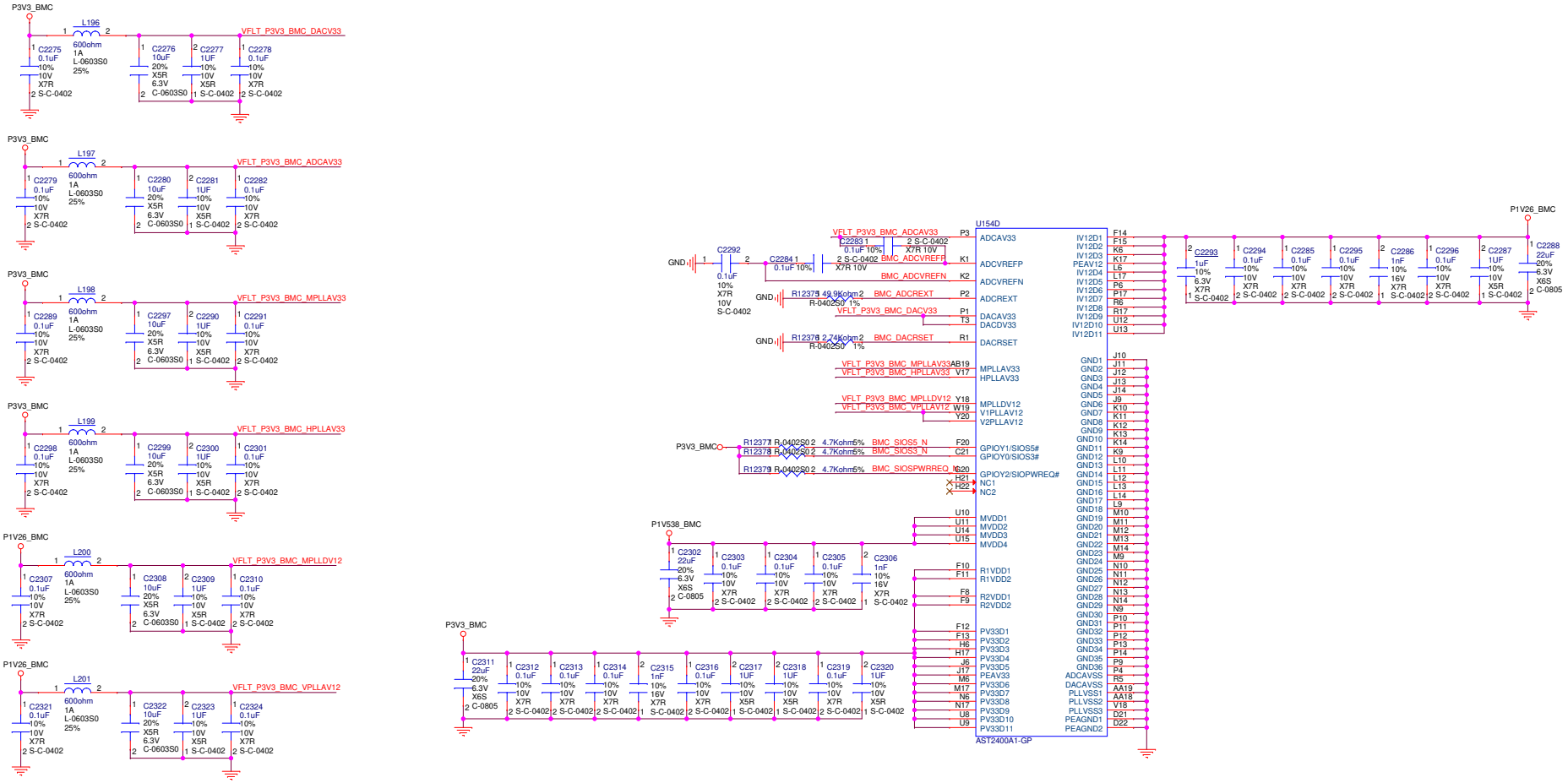
ufiSpace
UfiSpace Co., Ltd.

Title

58. BMC_AST2400_RGMII&SPI&USB

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BMC_AST2400_PWR & GND



ufiSpace

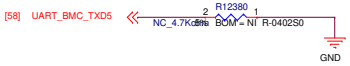
UfiSpace Co., Ltd.

Title: 59. BMC_AST2400_PWR & GND

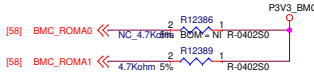
Document Number:	Sheet	Rev
PCB P/N: T99O089T03	59 of 77	

BMC_AST2400_HW_STRAPPING

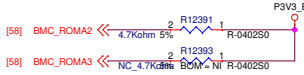
TXD5:Disable ARM ICE reset mode
0 : Enable ICE reset mode
1 : Disable ICE rest mode (default)



ROMA[1:0] : ARM CPU boot code selection
00 : Boot from NOR flash memory
01 : Boot from NAND flash memory
10 : Boot from SPI flash memory (default)
11 : Disable ARM CPU operation

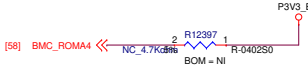


ROMA[3:2] : VGA memory size selection
00 : Select 8 MB VGA memory
01 : Select 16 MB VGA memory (default)
10 : Select 32 MB VGA memory
11 : Select 64 MB VGA memory



ROMA[4] : Boot flash memory extended option
NOR type flash: data bus width selection
0 : Select 8 bits interface
1 : Select 16 bits interface

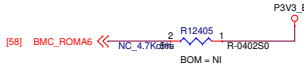
SPI type flash: boot address mode selection
0 : Boot with 24 bits address mode (default)
1 : Boot with 32 bits address mode



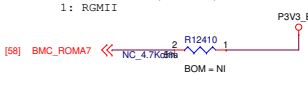
ROMA[5] : Enable VGA BIOS ROM
0 : No VGA BIOS ROM (for on-board application) (default)
1 : Enable VGA BIOS ROM (for add-on application)



ROMA[6] : Define MAC\#1 interface
0: RMII/NCSI (default)
1: RGMII



ROMA[7] : Define MAC\#2 interface
0: RMII/NCSI (default)
1: RGMII



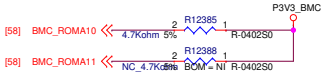
NTRST:Reserved



ROMA[9:8] : H-PLL default clock frequency selection
00: Select 384 MHz (default)
01: Select 360 MHz
10: Select 336 MHz
11: Select 204 MHz



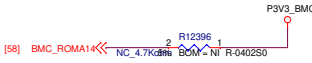
ROMA[11:10] : CPU/AHB clock frequency ratio selection
00 : Select CPU:AHB = 1:1
01 : Select CPU:AHB = 2:1 (default)
10 : Select CPU:AHB = 4:1
11 : Select CPU:AHB = 3:1



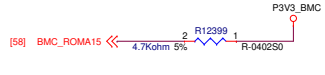
ROMA[13:12] : SPI mode selection
00 : Disable SPI interface (default)
01 : Enable SPI Master
10 : Enable SPI Master and SPI Slave to AHB Bridge
11 : Enable SPI Bypass



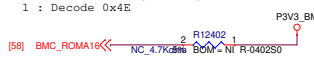
ROMA[14] : Enable LPC dedicated reset pin function
0 : LPC reset is shared with PCI reset pin. (default)
1 : LPC reset is shared with GPIOB4.



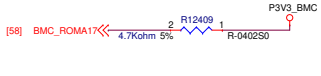
ROMA[15] : VGA Class Code selection
0 : Select the Class Code for video device
1 : Select the Class Code for VGA device (default)



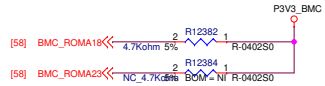
ROMA[16] : SuperIO configuration address selection
0 : Decode 0x2E (default)
1 : Decode 0x4E



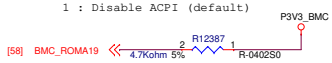
ROMA[17] : Enable BMC 2nd boot watchdog timer
0 : Disable
1 : Enable BMC 2nd boot watchdog timer start
counting at power up.
The watchdog timer was located at WDT2.
After watchdog timeout, it will reset BMC
and restart booting from the 2nd boot flash
at CS1#. CS1# must be the same flash type
as CS0# and could be the same firmware as CS0#. (default)



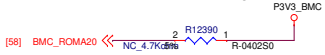
ROMA[23:18] : Clock source selection
00 : 24 MHz CLKIN
01 : 48 MHz CLKIN (default)
10 : 25MHz CLKIN,24MHz USBCKI
11 : 25MHz CLKIN,48MHz USBCKI



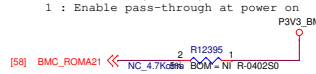
ROMA[19] : Disable ACPI function
0 : Enable ACPI
1 : Disable ACPI (default)



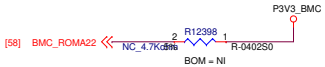
ROMA[20] : Disable LPC to decode SuperIO 0x2E/0x4E address
0 : Enable address decoding (default)
1 : Disable address decoding



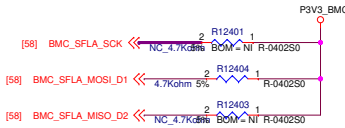
ROMA[21] : Enable GPIOD pass-through mode
0 : Disable (default)
1 : Enable pass-through at power on



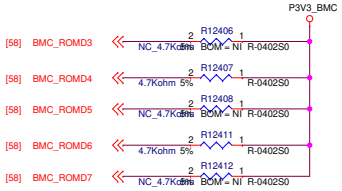
ROMA[22] : Enable GPIOE pass-through mode
0 : Disable (default)
1 : Enable pass-through at power on

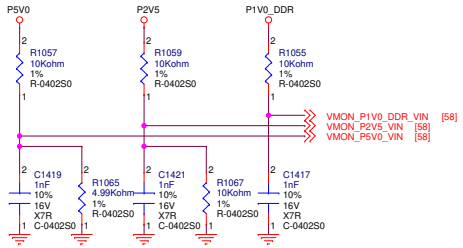


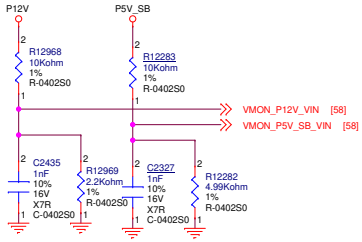
ROMD[2:0]:010:DDR3 SDRAM with CL=6,CWL=5

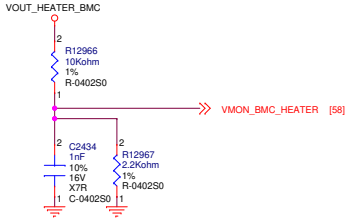


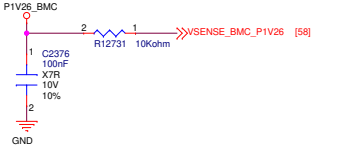
ROMD[7:3] : Reserved for Software DRAM type selection

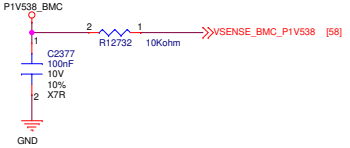


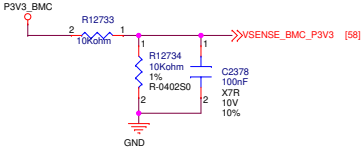










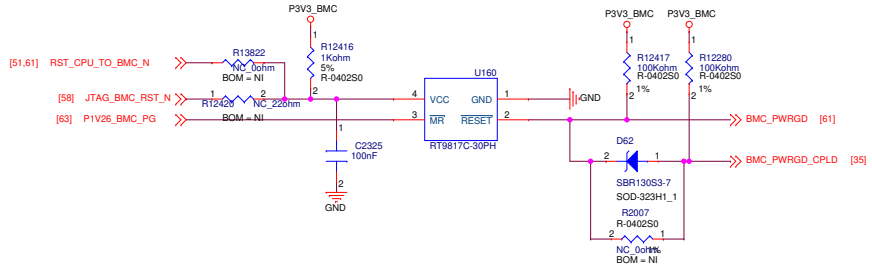


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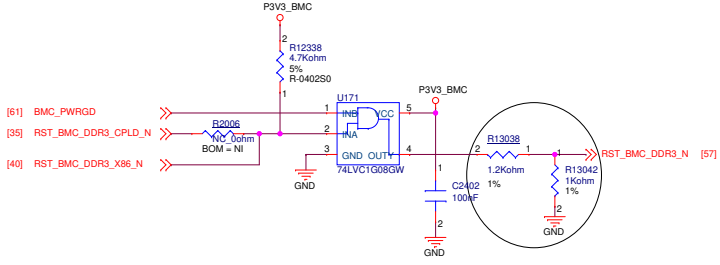
Title
60. BMC_AST2400_HW_STRAPPING

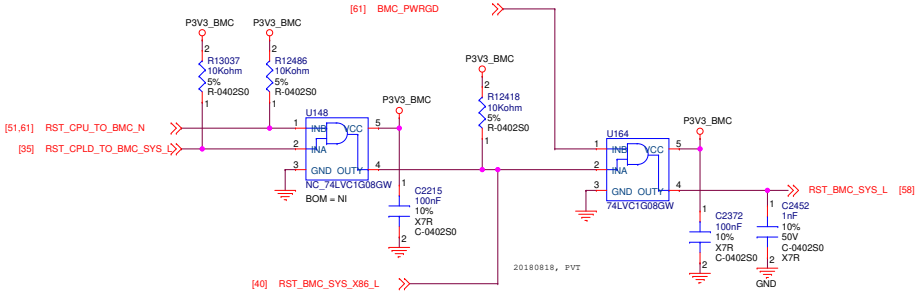
Document Number:		Sheet	Rev
PCB P/N:	T99O089T03	60 of 77	

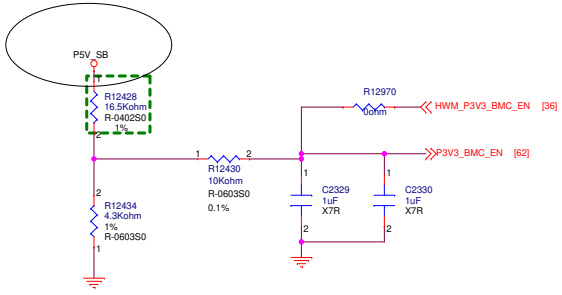
BMC_PWR SEQUENCE & RESET

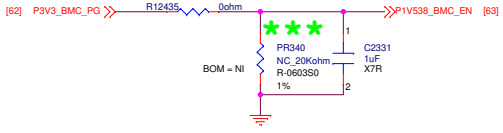


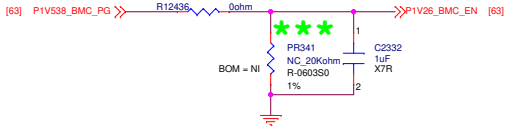
RT9817 is push pull type
with 220ms delay











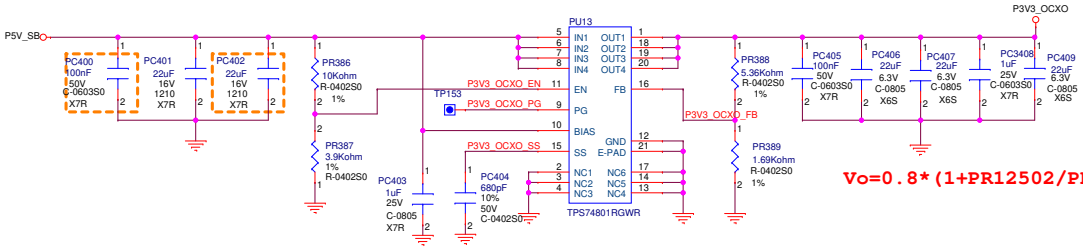
ufiSpace
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Title
61. BMC_PWR SEQUENCE & RESET

Document Number: PCB P/N:	Sheet	Rev
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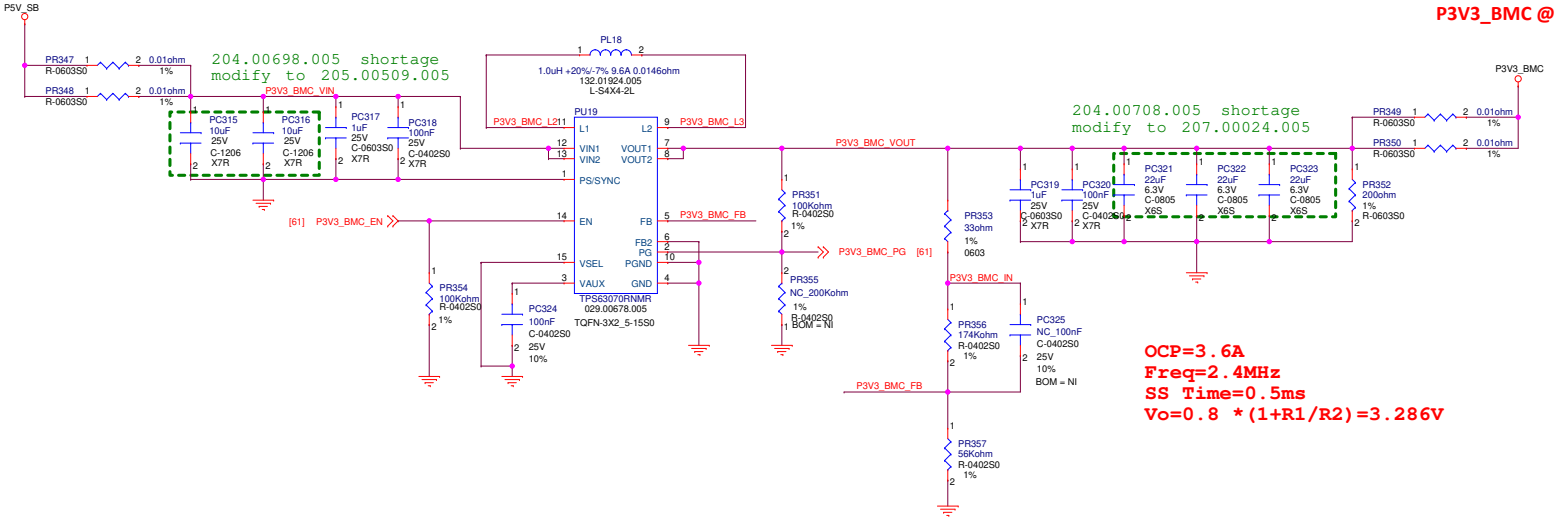
BMC_PWR_5VSTB TO 3.3V

P3V3_OCXO @ 1A



Vo=0.8*(1+PR12502/PR12499)=3.33V

P3V3_BMC @ 0.83A



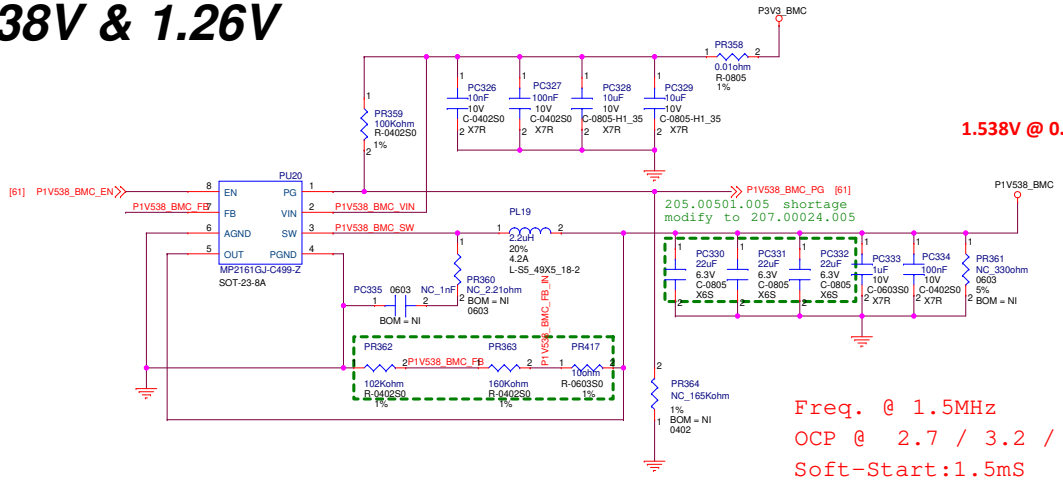
OCP=3.6A
Freq=2.4MHz
SS Time=0.5ms
Vo=0.8 *(1+R1/R2)=3.286V

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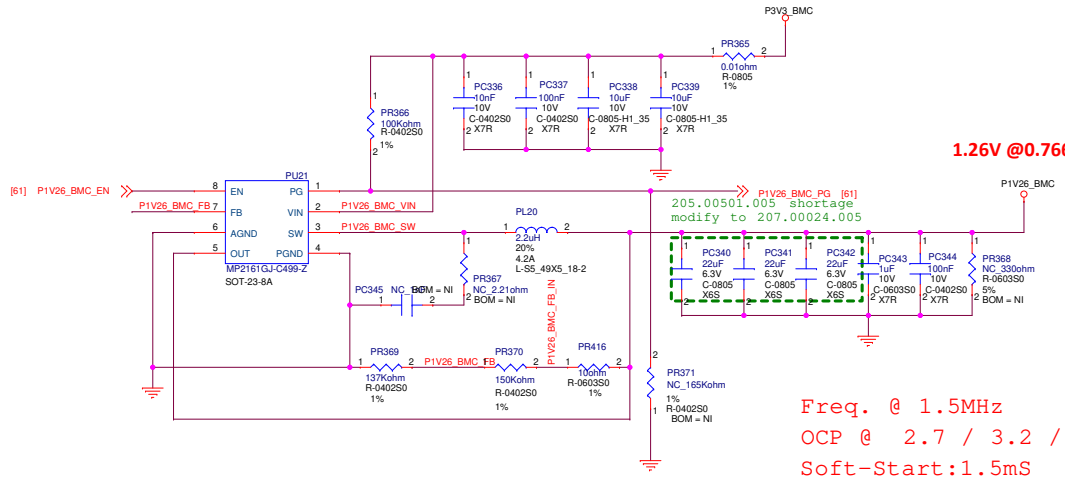
Title: 62. BMC_DC_5VSTB TO 3.3V

Document Number: PCB P/N: T99O089T03	Sheet 62 of 77	Rev

BMC_DC_3.3V TO 1.538V & 1.26V



Freq. @ 1.5MHz
OCP @ 2.7 / 3.2 / 4.0 A
Soft-Start:1.5mS
1.538V @ 0.452A
Vo=0.6*(1+PR363/PR362)=1.538V



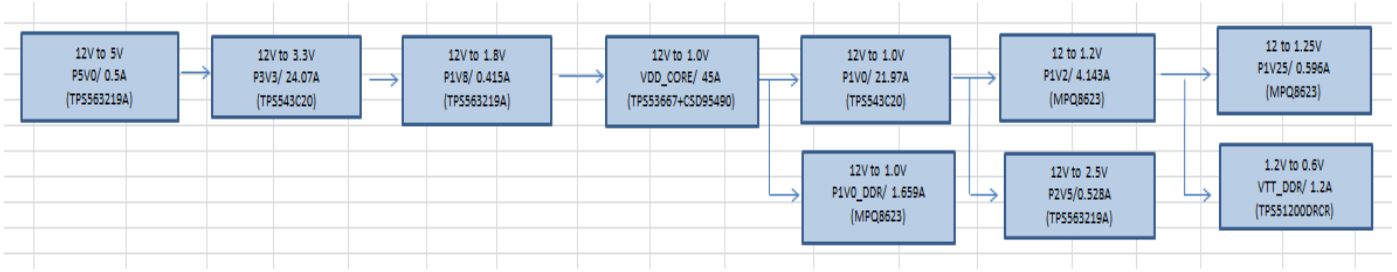
Freq. @ 1.5MHz
OCP @ 2.7 / 3.2 / 4.0 A
Soft-Start:1.5mS
1.26V @0.766A
Vo=0.6*(1+PR370/PR369)=1.257V

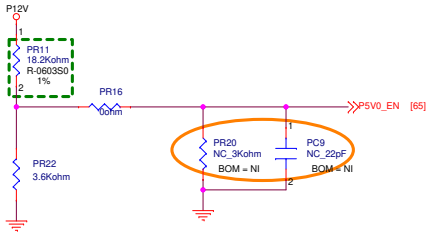
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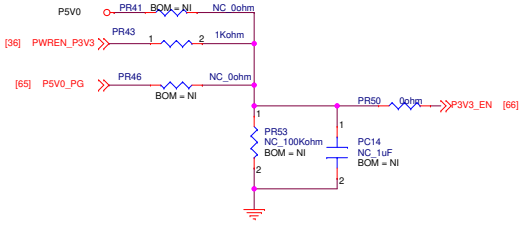
Title
63. BMC_DC_3.3V TO 1.5V & 1.26V

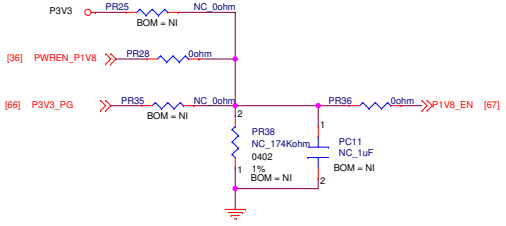
Document Number: PCB P/N: T99O089T03	Sheet 63 of 77	Rev

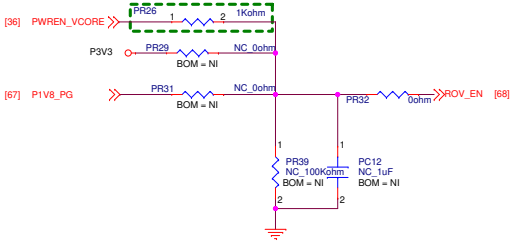
DC_PWR UP SEQUENCE





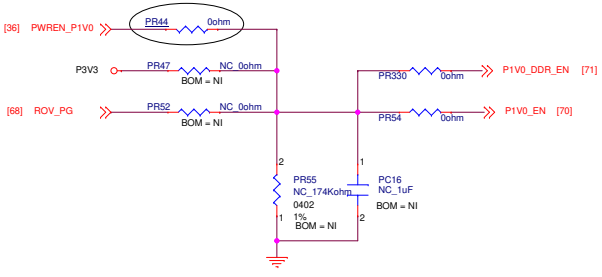


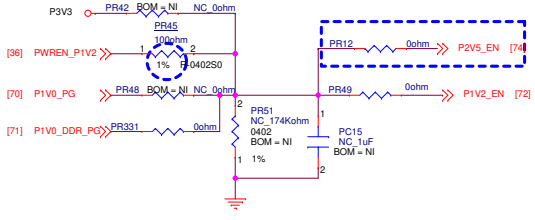




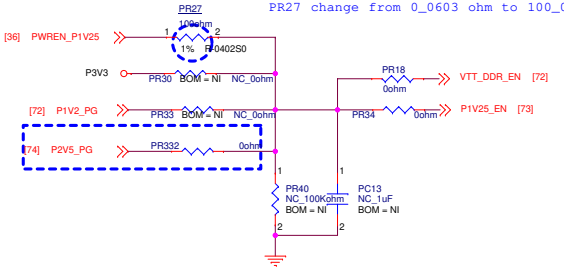
EE note: 20200504
modify P2V5_EN circuit for P2V5 Sequence modify

EE note: 20200504
PR27 change from 0_0603 ohm to 100_0402 ohm

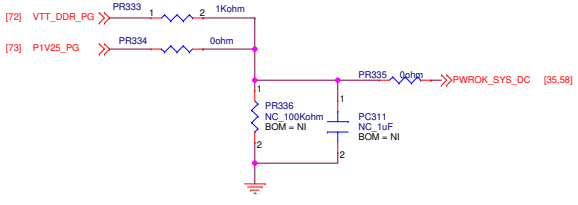




EE note: 20200504
PR45 change from 0_0603 ohm to 100_0402 ohm



EE note: 20200504
modify P2V5_PG circuit for next power rail Enable Sequence modify



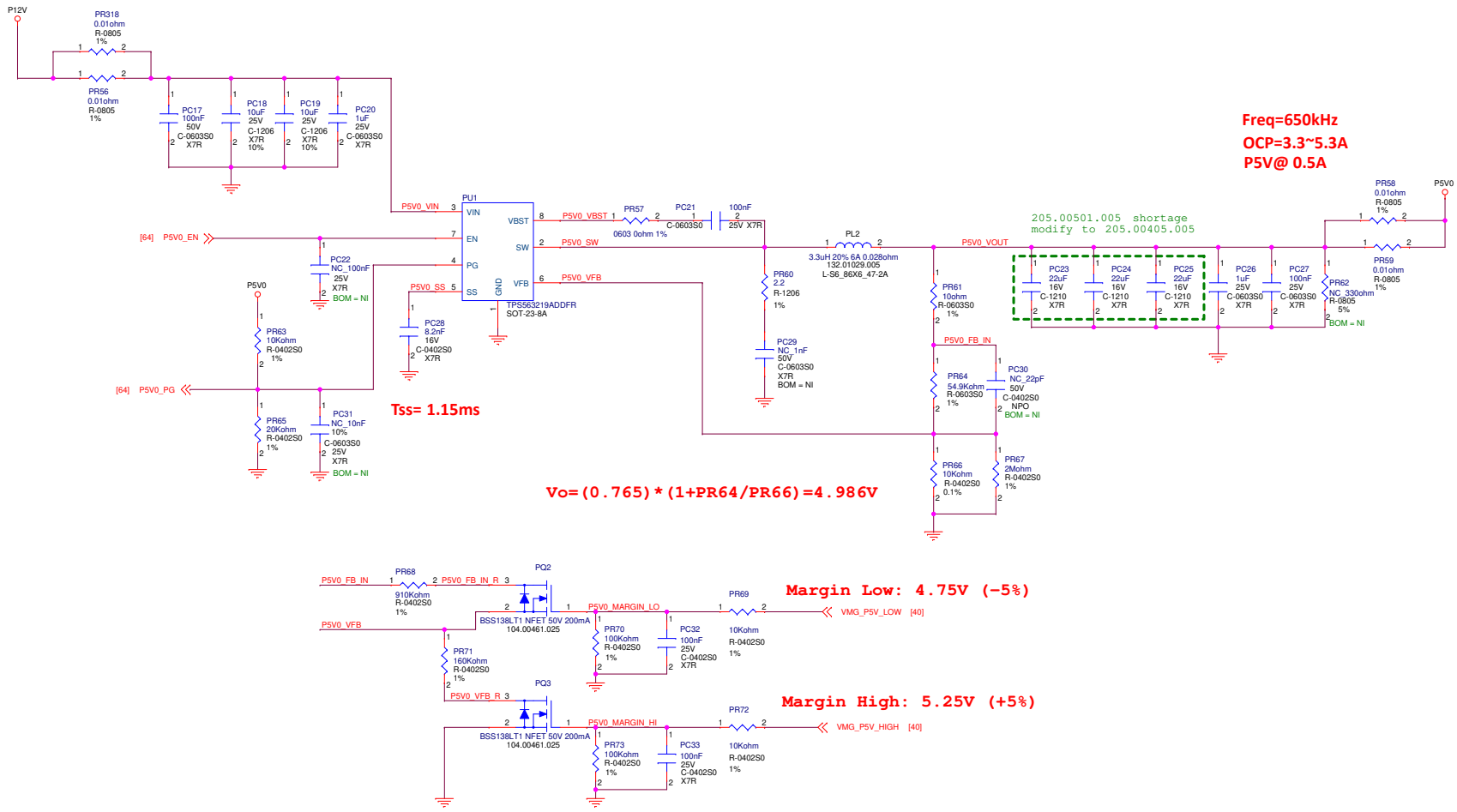
<Core Design>

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Title
64. DC_PWR UP SEQUENCE

Document Number: PCB P/N:	Sheet	Rev
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DC_PWR_12V TO 5V



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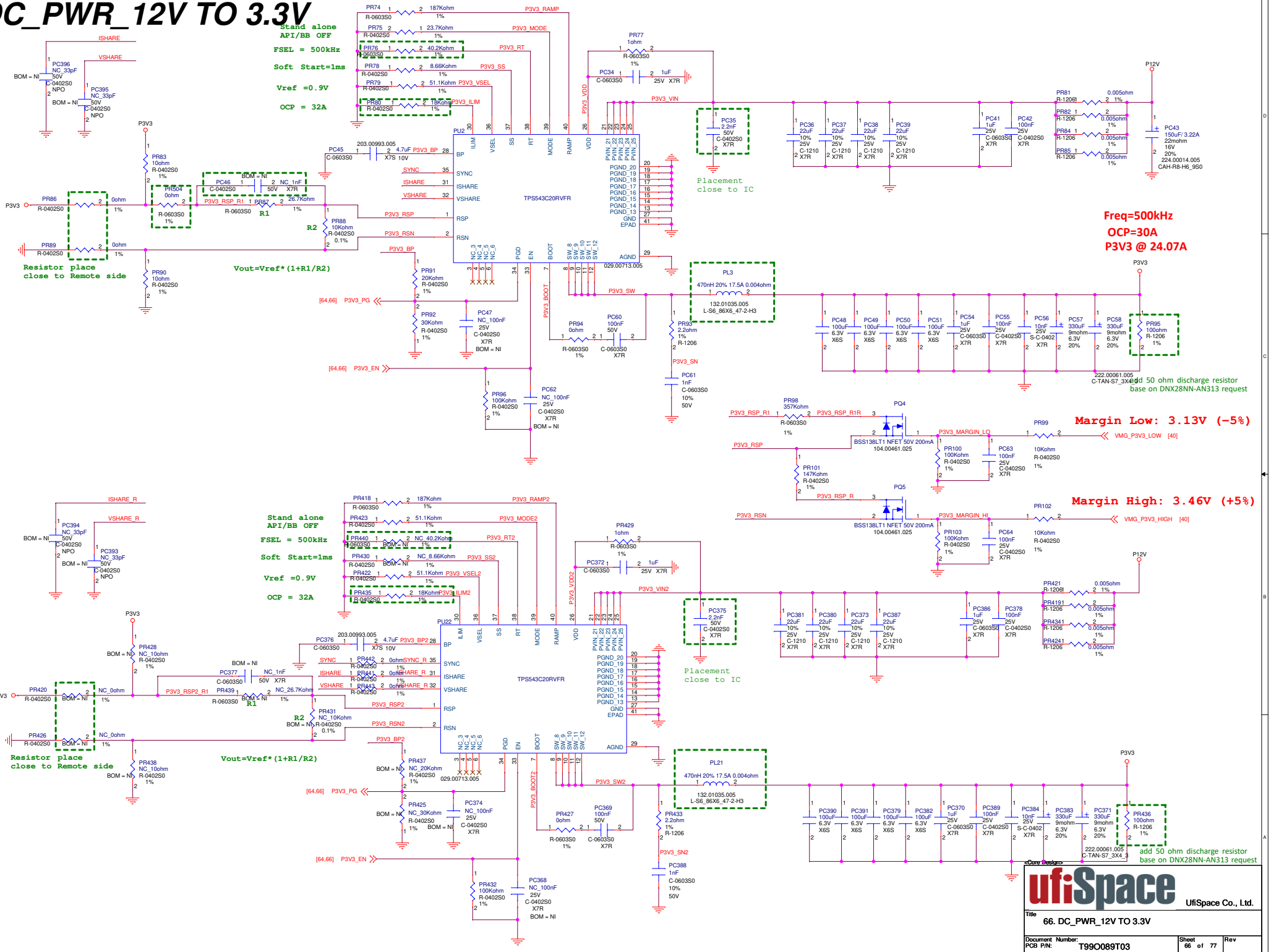
Title: 65. DC_PWR_12V TO 5V

Document Number: PCB P/N: T99O089T03

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Rev

DC_PWR_12V TO 3.3V



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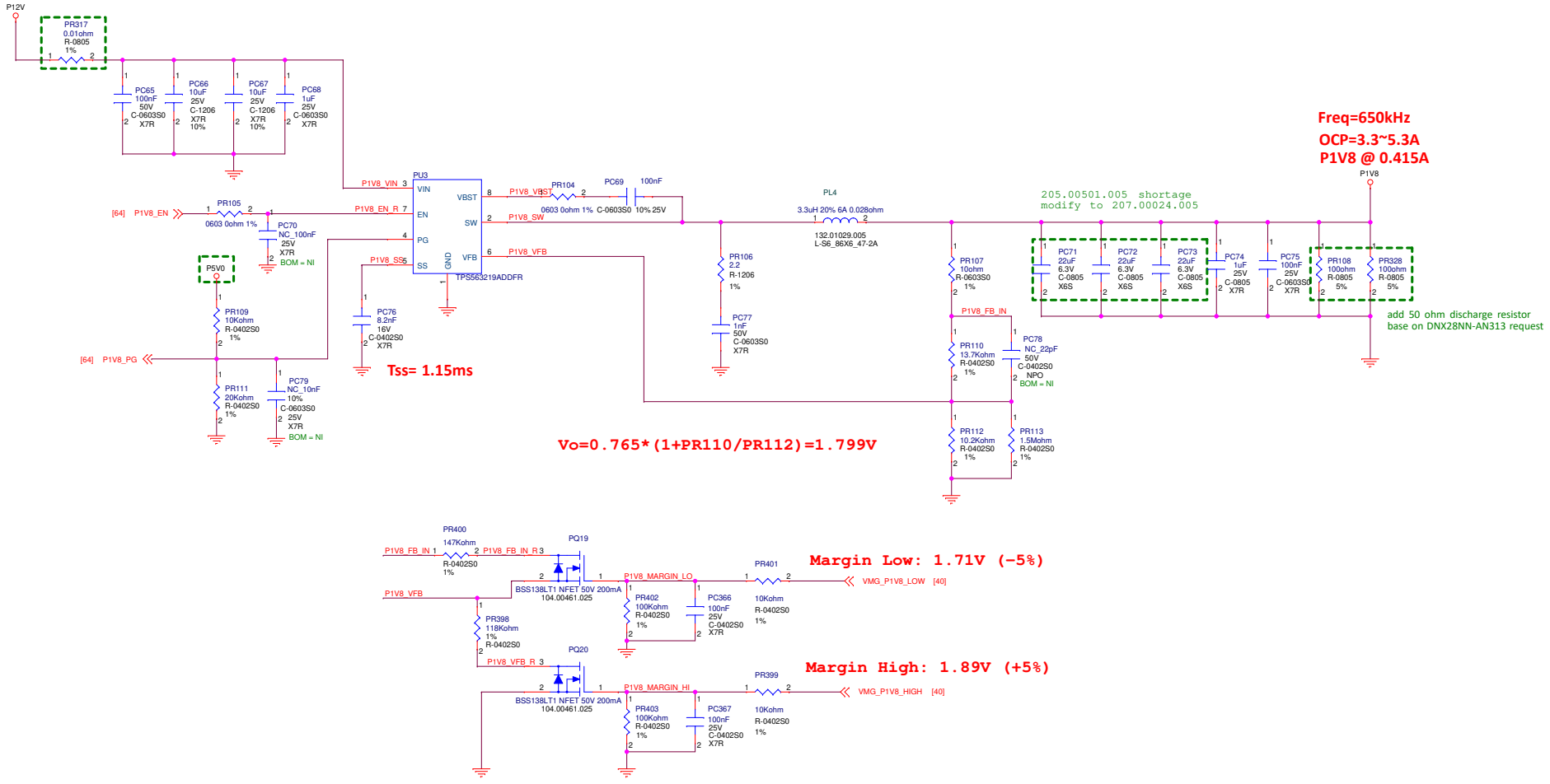
Title: 66. DC_PWR_12V TO 3.3V

Document Number: PCB P/N: T99O089T03

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Rev

DC_PWR_12V TO 1.8V



<Core Design>

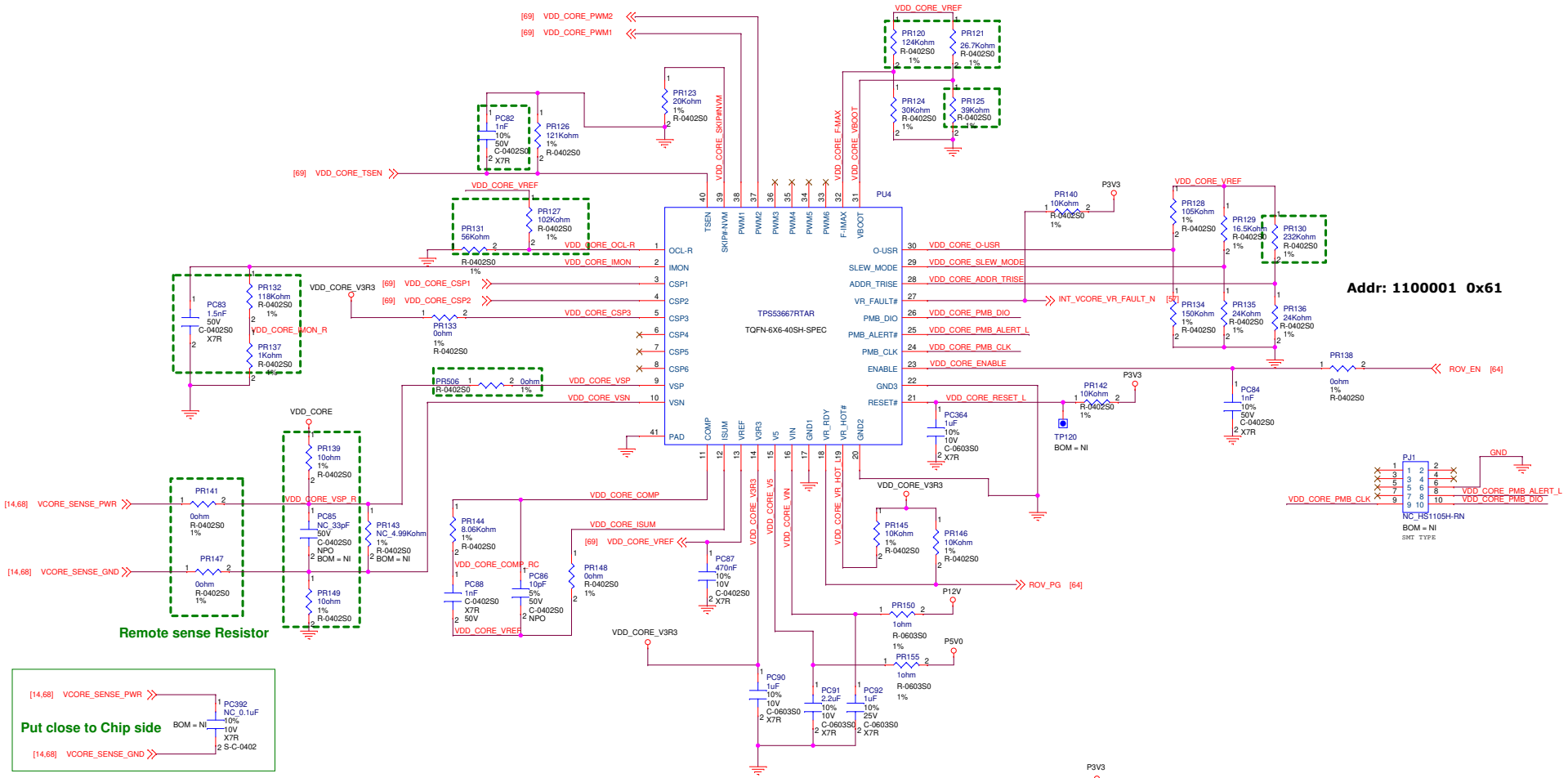
UfiSpace Co., Ltd.

Title: 67. DC_PWR_12V TO 1.8V

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DC_PWR_12V TO VCORE_CNTRL

VCORE CONTROLLER



1. ICC_MAX = 50A (F-IMAX to VREF R is 123k)
2. Freq = 500kHz (F-IMAX to GND R is 30kohm)
3. OC_FAULT_LIMIT=62.5A (Value is ICCmax *1.25)
3. Per-Phase OCL is 36A (OCL-R to GND R is 56kohm)
4. RAMP LEVEL is 150mV (OCL-R to VREF V is 102kohm)
5. VR12.0 (VBOOT to VREF is 26.7kohm)
   VBOOT=1.0V (VBOOT to GND is 39kohm)
   Zero Load-line: RISUM=0ohm
   Vout slew rate is 0.68mV/us; SS=1.47ms
   PMBUS Address: 1100001 (0x61)

<Core Design>

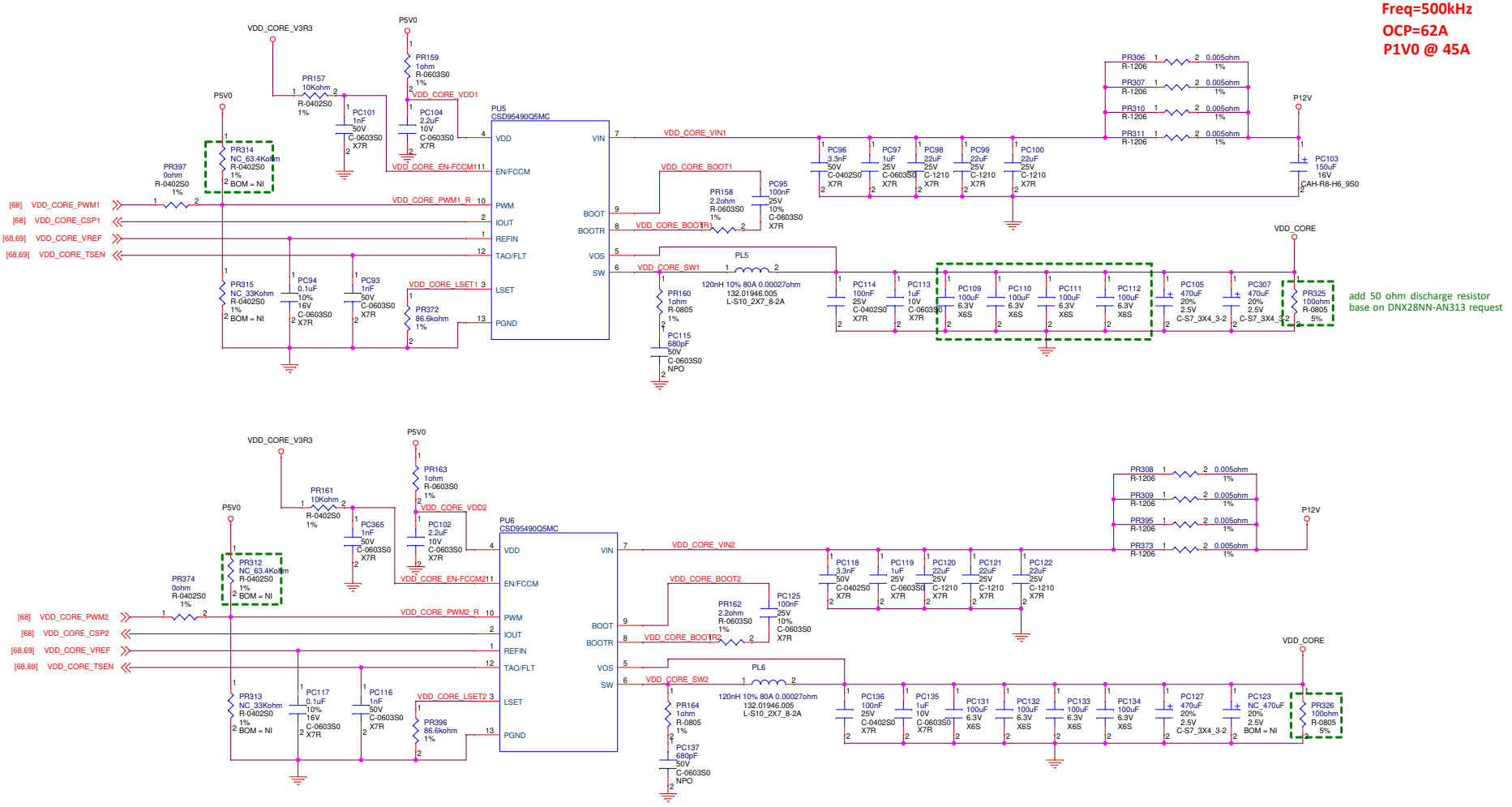
UfiSpace Co., Ltd.

Title: 68. DC_PWR_12V TO VCORE_CNTRL

Document Number: T99O089T03 | Sheet 68 of 77 | Rev

DC_PWR_12V TO VCORE_DRVR

Freq=500kHz
OCP=62A
P1V0 @ 45A

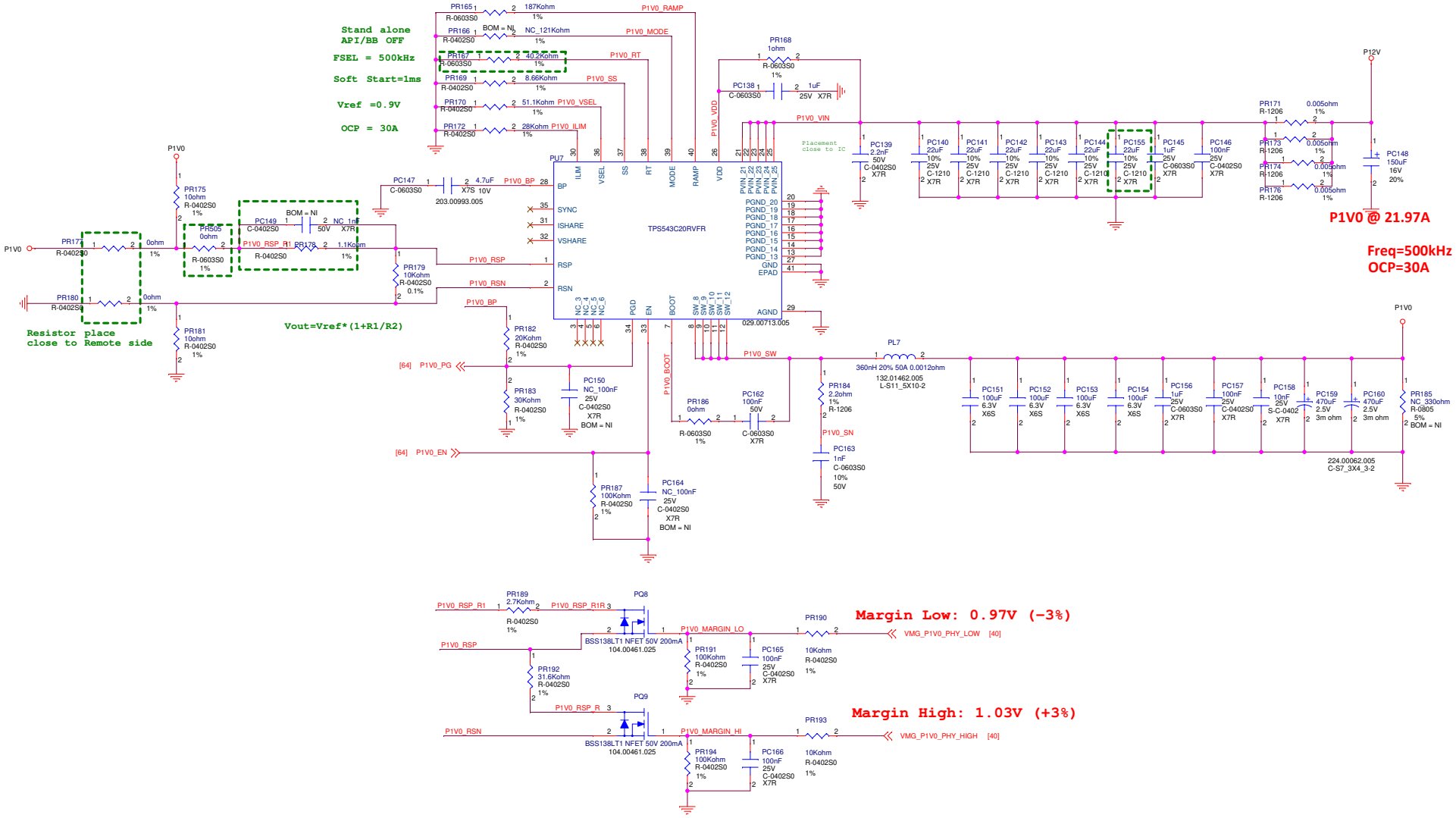


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Title
69. DC_PWR_12V TO VCORE_DRVR

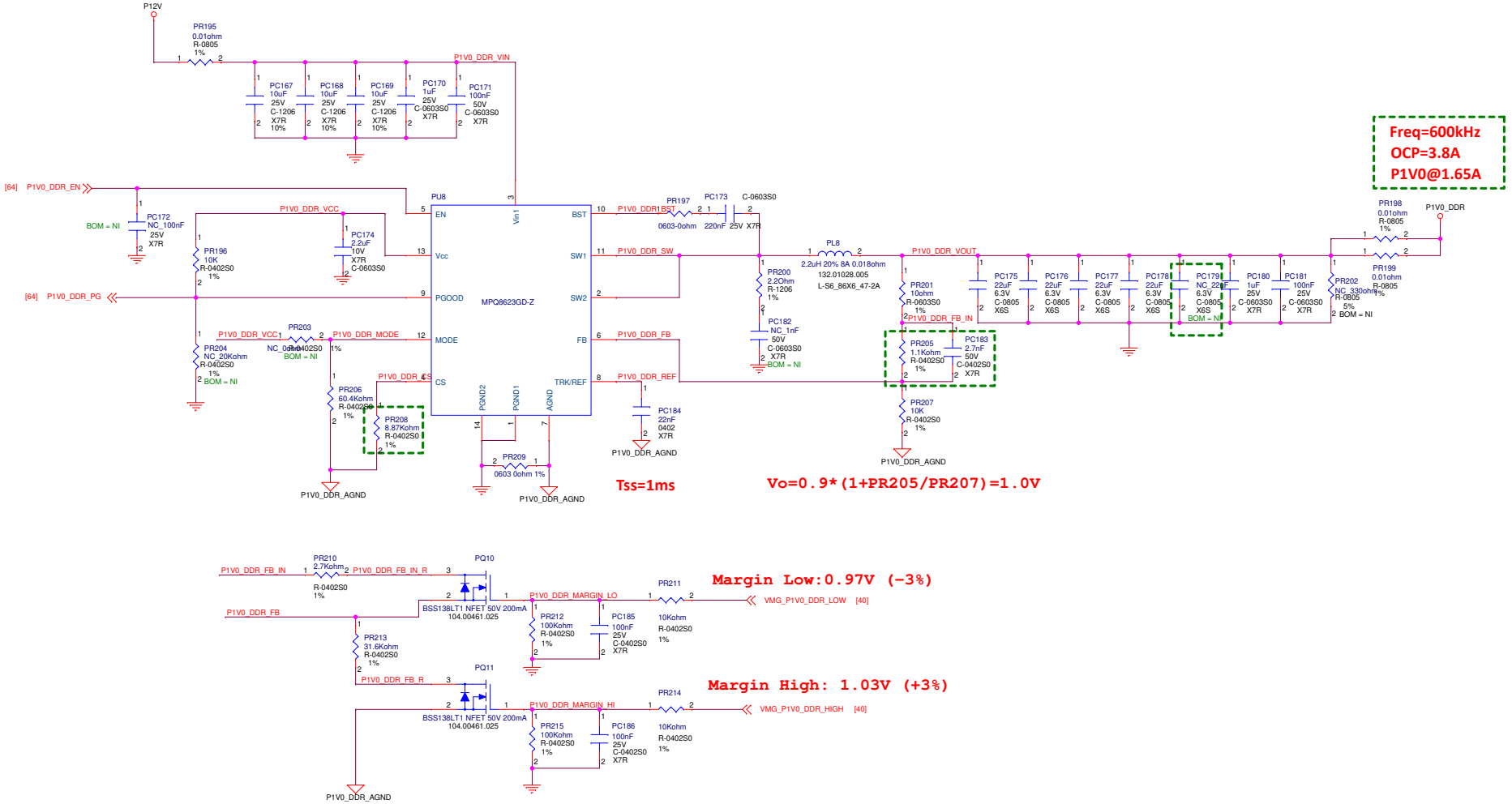
Document Number: PCB P/N: T99O089T03	Sheet 69 of 77	Rev

DC_PWR_12V TO 1.0V



UfiSpace Co., Ltd.	
Title	70. DC_PWR_12V TO 1.0V
Document Number: PCB P/N:	T99O089T03
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Rev	

DC_PWR_12V TO 1.0V

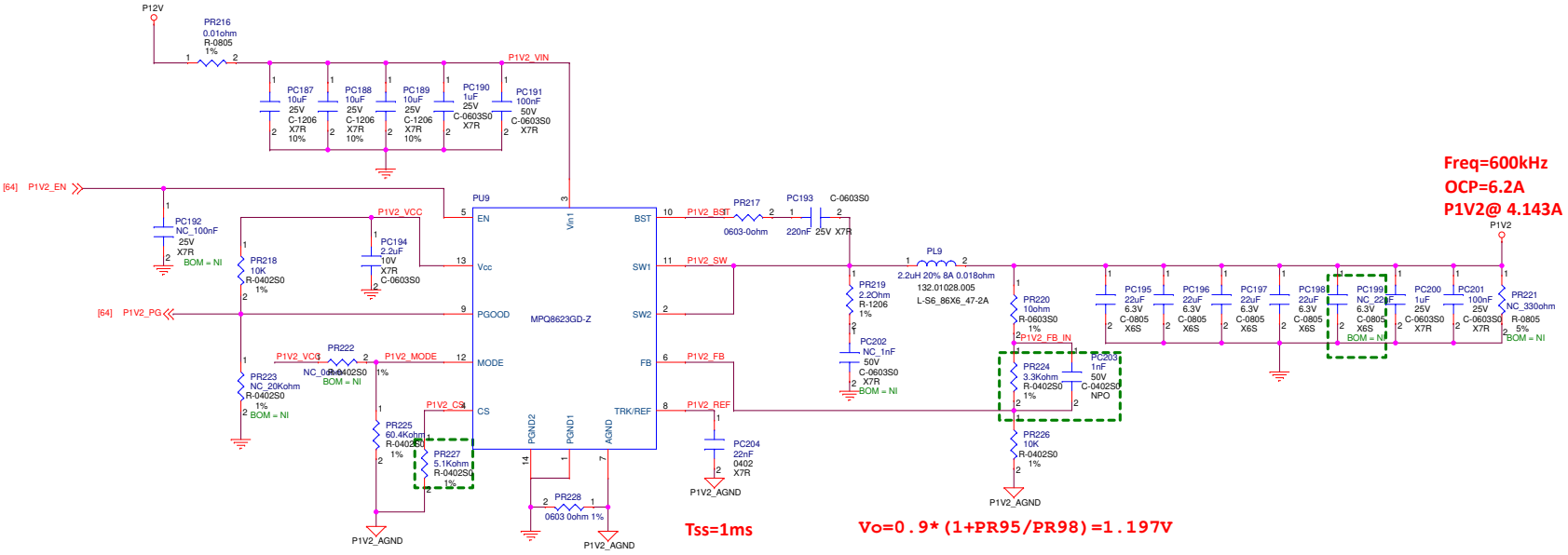


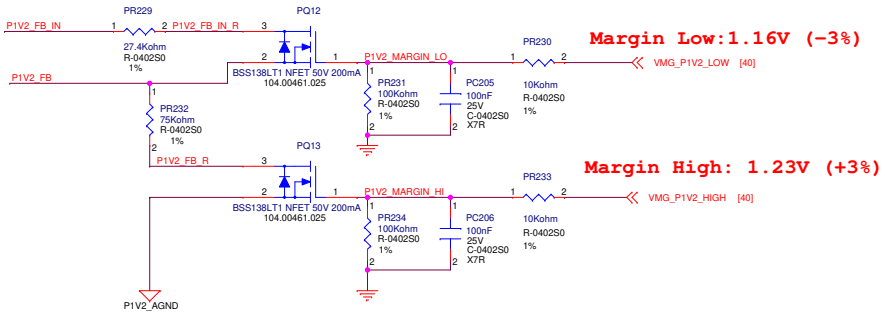
ufiSpace UfiSpace Co., Ltd.

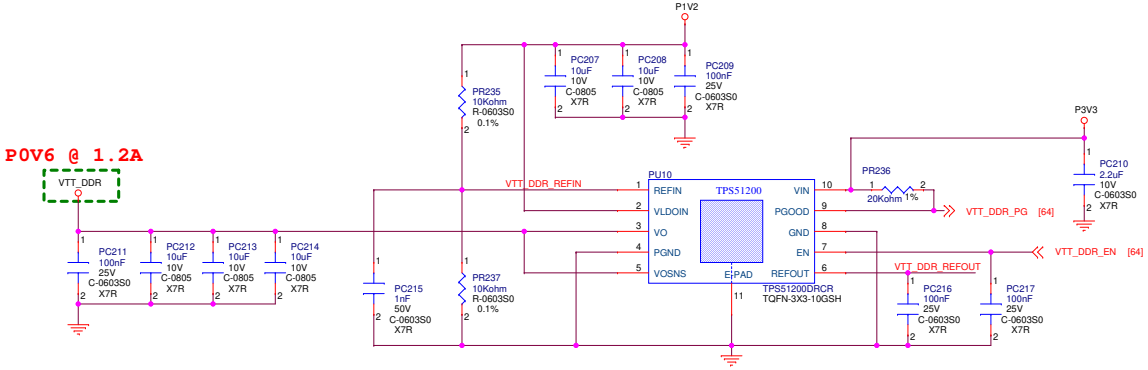
Title: 71. DC_PWR_12V TO 1.0V_DDR

Document Number: PCB P/N:	Sheet	Rev
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DC_PWR_12V TO 1.2V & 0.6V





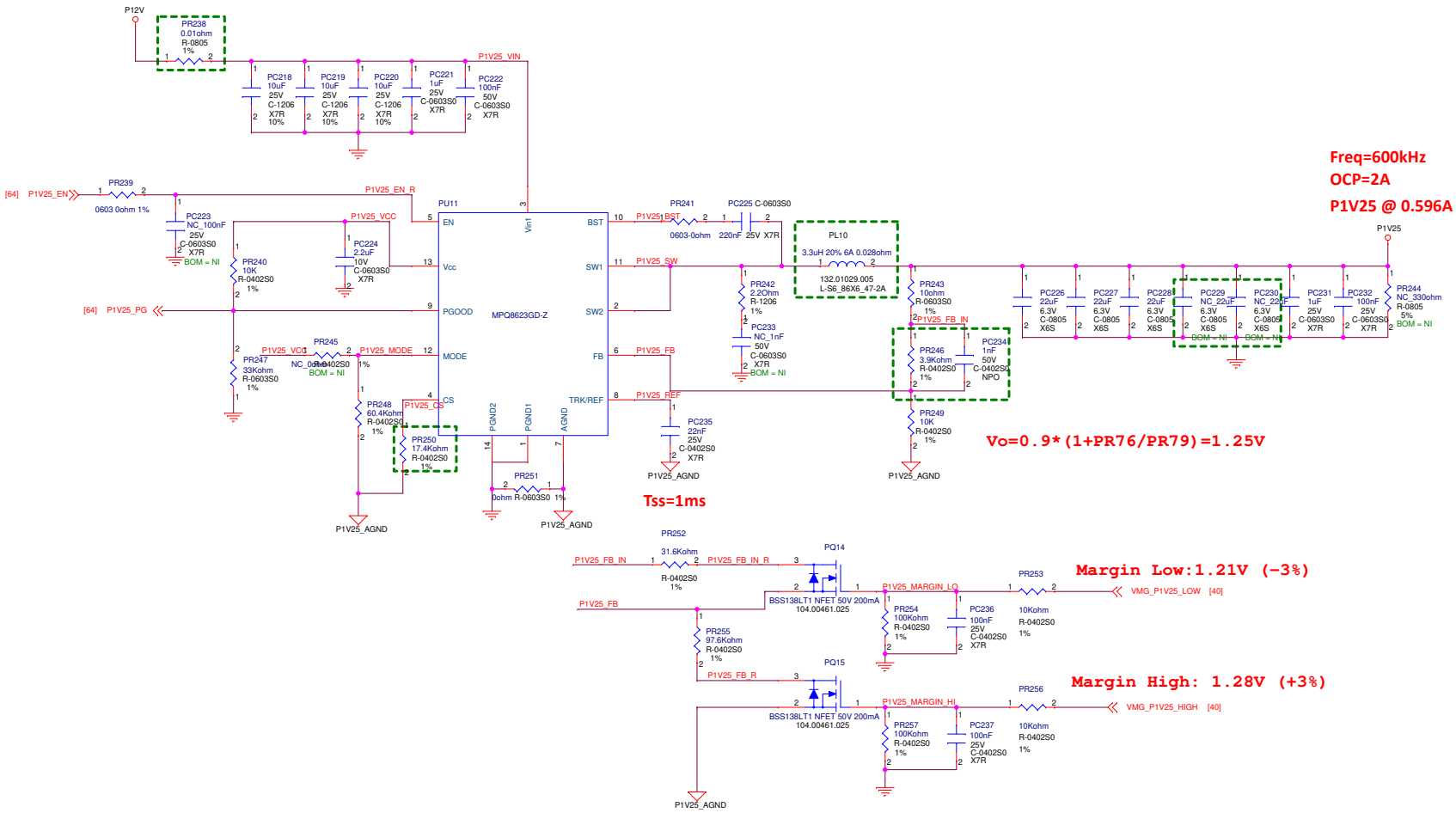


ufiSpace UfiSpace Co., Ltd.

Title: 72. DC_PWR_12V TO 1.2V & 0.6V

Document Number:	Sheet	Rev
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DC_PWR_12V TO 1.25V



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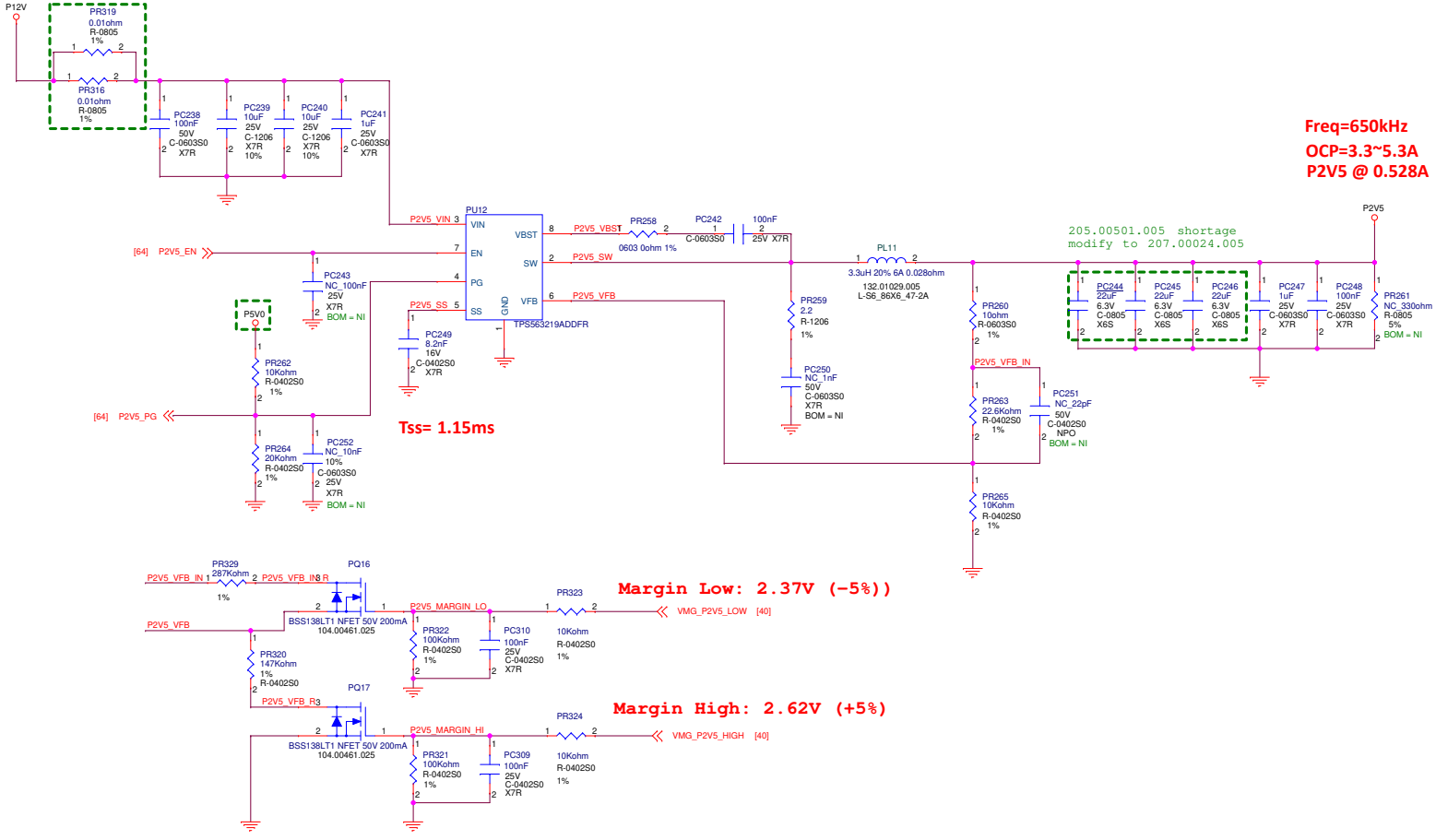
Title: 73. DC_PWR_12V TO 1.25V

Document Number: PCB P/N: T99O089T03

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Rev

DC_PWR_12V TO 2.5V



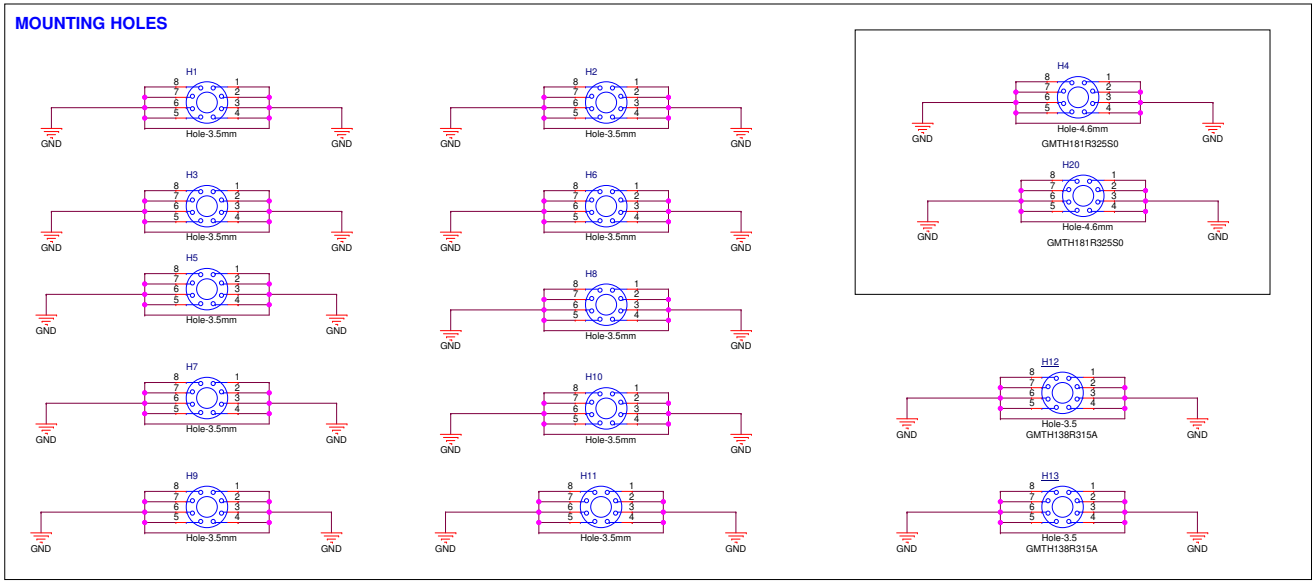
ufiSpace UfiSpace Co., Ltd.

Title: 74. DC_PWR_12V TO 2.5V

Document Number: T99O089T03 | Sheet 74 of 77 | Rev

HOLES & BOM ONLY PARTS

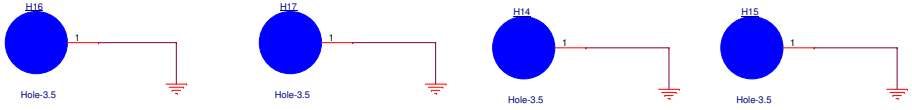
MOUNTING HOLES



PHY's HEATSINK HOLES

remove 100G PHY Heatsink Holes

MAC's HEATSINK HOLES



BOM ONLY PARTS

Heat sink,Sheild Frame/Cover ,PCB, Label

SN_LABEL
503.00899.005
SN LABEL
SN Label

PCB
304.01020.005U
PCB Rev. 005
PCB

BMC_LABEL
***JS5008
BMC LABEL
NC_Legal Fee Sticker
BOM = NI

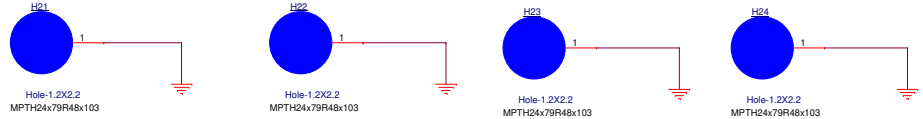
HEATER
310.00138.005U
5-5.5 OHM
BMC HEATER
Heater

HS
400.00747.015
FOR BCM54140
NC_HS_PHY_1G
BOM = NI

SHIELDING_COVER
426.05394.015
OCXO SHIELDING COVER
SHIELDING COVER

SHIELDING_FRAME
432.00718.015
OCXO SHIELDING FRAME
SHIELDING FRAME

OCXO SHIELDING COVER HOLES



<Core Design>

UfiSpace Co., Ltd.

Title: 75. HOLES & BOM ONLY PARTS

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